



LIST OF FIGURES

Chapter 1

Figure 1-1.	SCC Block Diagram	1-4
Figure 1-2.	Z85X30 Pin Functions	1-5
Figure 1-3.	Z80X30 Pin Functions	1-6
Figure 1-4.	Z85X30 DIP Pin Assignments	1-6
Figure 1-5.	Z85X30 PLCC Pin Assignments	1-6
Figure 1-6.	Z80X30 DIP Pin Assignments	1-7
Figure 1-7.	Z80X30 PLCC Pin Assignments	1-7

Chapter 2

Figure 2-1.	Z80X30 Read Cycle	2-2
Figure 2-2.	Z80X30 Write Cycle	2-3
Figure 2-3.	Z80X30 Interrupt Acknowledge Cycle	2-4
Figure 2-4.	Write Register 7 Prime (WR7')	2-8
Figure 2-5.	Z85X30 Read Cycle Timing	2-10
Figure 2-6.	Z85X30 Write Cycle Timing	2-11
Figure 2-7.	Z85X30 Interrupt Acknowledge Cycle Timing	2-11
Figure 2-8a.	Write Register 7 Prime (WR7') for the 85230	2-14
Figure 2-8b.	Write Register 7 Prime for the 85C30	2-14
Figure 2-9.	ESCC Interrupt Sources	2-16
Figure 2-10.	Peripheral Interrupt Structure	2-17
Figure 2-11.	Internal Priority Resolution	2-17
Figure 2-12.	RR3 Interrupt Pending Bits	2-18
Figure 2-13.	Interrupt Flow Chart (for each interrupt source).	2-20
Figure 2-14.	Write Register 1 Receive Interrupt Mode Control	2-22
Figure 2-15.	Special Conditions Interrupt Service Flow	2-24
Figure 2-16.	Transmit Interrupt Status When WR7' D5=1 For ESCC	2-26
Figure 2-17.	Transmit Buffer Empty Bit Status For ESCC For Both WR7' and WR7' D5=0	2-27
Figure 2-18.	Transmit Interrupt Status When WR7' D5=0 For ESCC	2-27
Figure 2-19.	TxIP Latching on the ESCC	2-27
Figure 2-20.	Operation of TBE, Tx Underrun/EOM and TxIP on NMOS/CMOS.	2-28
Figure 2-21.	Operation of TBE, Tx Underrun/EOM and TxIP on ESCC	2-29
Figure 2-22.	Flowchart example of processing an end of packet	2-30
Figure 2-23.	RR0 External/Status Interrupt Operation	2-31
Figure 2-24.	Wait On Transmit Timing	2-34
Figure 2-25.	Wait On Transmit Timing	2-34
Figure 2-26.	Wait On Receive Timing	2-35

Figure 2-27.	Wait On Receive Timing	2-35
Figure 2-28.	Transmit Request Assertion	2-36
Figure 2-29.	Z80X30 Transmit Request Release	2-37
Figure 2-30.	Z85X30 Transmit Request Release	2-37
Figure 2-31.	/DTR//REQ Deassertion Timing	2-38
Figure 2-32.	DMA Receive Request Assertion	2-39
Figure 2-33.	Z80X30 Receive Request Release	2-40
Figure 2-34.	Z85X30 Receive Request Release	2-40
Figure 2-35.	Local Loopback	2-41
Figure 2-36.	Auto Echo	2-41

Chapter 3

Figure 3-1.	Baud Rate Generator	3-1
Figure 3-2.	Baud Rate Generator Start Up	3-2
Figure 3-3.	Data Encoding Methods	3-4
Figure 3-4.	Manchester Encoding Circuit	3-6
Figure 3-5.	Digital Phase-Locked Loop	3-7
Figure 3-6.	DPLL in NRZI Mode	3-8
Figure 3-7.	DPLL Operating Example (NRZI Mode)	3-9
Figure 3-8.	DPLL Operation in the FM Mode	3-9
Figure 3-9.	DPLL Transmit Clock Counter Output (ESCC only)	3-11
Figure 3-10.	Clock Multiplexer	3-12
Figure 3-11.	Async Clock Setup Using an External Crystal	3-13
Figure 3-12.	Clock Source Selection	3-13
Figure 3-13.	Synchronous Transmission, 1x Clock Rate, FM Data Encoding, using DPLL	3-14

Chapter 4

Figure 4-1.	Transmit Data Path	4-1
Figure 4-2.	Receive Data Path	4-2
Figure 4-3.	Asynchronous Message Format	4-3
Figure 4-4.	Monosync Data Character Format	4-8
Figure 4-5.	Sync Character Programming	4-11
Figure 4-6.	/SYNC as an Input	4-11
Figure 4-7.	/SYNC as an Output	4-12
Figure 4-8.	Changing Character Length	4-13
Figure 4-9.	Receive CRC Data Path	4-14
Figure 4-10.	Transmitter to Receiver Synchronization	4-17
Figure 4-11.	SDLC Message Format	4-18
Figure 4-12.	/SYNC as an Output	4-23
Figure 4-13.	Changing Character Length	4-24
Figure 4-14.	Residue Code 101 Interpretation	4-25
Figure 4-15.	SDLC Frame Status FIFO (N/A on NMOS)	4-28
Figure 4-16.	SDLC Byte Counting Detail	4-29

Chapter 5

Figure 5-1.	Write Register 0 in the Z85X30	5-3
Figure 5-2.	Write Register 0 in the Z80X30	5-3
Figure 5-3.	Write Register 1	5-4
Figure 5-4.	Write Register 2	5-7
Figure 5-5.	Write Register 3	5-7

Figure 5-6.	Write Register 4	5-8
Figure 5-7.	Write Register 5	5-9
Figure 5-8.	Write Register 6	5-11
Figure 5-9.	Write Register 7	5-11
Figure 5-10.	Write Register 7 Prime	5-12
Figure 5-10a.	Write Register 7 Prime (WR7')	5-13
Figure 5-11.	Write Register 9	5-14
Figure 5-12.	Write Register 10	5-15
Figure 5-13.	NRZ (NRZI), FM1 (FM0) Timing	5-16
Figure 5-14.	Write Register 11	5-17
Figure 5-15.	Write Register 12	5-18
Figure 5-16.	Write Register 13	5-19
Figure 5-17.	Write Register 14	5-19
Figure 5-18.	Write Register 15	5-20
Figure 5-19.	Read Register 0	5-21
Figure 5-20.	Read Register 1	5-23
Figure 5-21.	Read Register 2	5-25
Figure 5-22.	Read Register 3	5-25
Figure 5-23.	Read Register 6 (Not on NMOS)	5-25
Figure 5-24.	Read Register 7 (Not on NMOS)	5-26
Figure 5-25.	Read Register 10	5-26
Figure 5-26.	Read Register 12	5-27
Figure 5-27.	Read Register 13	5-27
Figure 5-28.	Read Register 15	5-27