

CHAPTER 5

REGISTER DESCRIPTIONS

5.1 INTRODUCTION

This section describes the functions of the various bits in the registers of the SCC (Tables 5-1 and 5-2). Reserved bits are not used in this implementation of the device and may or may not be physically present in the device. For the register addresses, also refer to Tables 2-1, 2-2 and 2-5 in Chapter 2. Reserved bits that are physically present are

readable and writable but reserved bits that are not present will always be read as zero. To ensure compatibility with future versions of the device, reserved bits should always be written with zeros. Reserved commands are not used for the same reason.

Table 5-1. SCC Write Registers

Reg	Description
WR0	Reg. pointers, various initialization commands
WR1	Transmit and Receive interrupt enables, WAIT/DMA commands
WR2	Interrupt Vector
WR3 ²	Receive parameters and control modes
WR4 ²	Transmit and Receive modes and parameters
WR5 ²	Transmit parameters and control modes
WR6	Sync Character or SDLC address
WR7	Sync Character or SDLC flag
WR7 ¹	Extended Feature and FIFO Control (WR7 Prime)
WR8	Transmit buffer
WR9	Master Interrupt control and reset commands
WR10 ²	Miscellaneous transmit and receive control bits
WR11	Clock mode controls for receive and transmit
WR12	Lower byte of baud rate generator
WR13	Upper byte of baud rate generator
WR14	Miscellaneous control bits
WR15	External status interrupt enable control

Notes for Tables 5-1 and 5-2:

1. ESCC and 85C30 only.
2. On the ESCC and 85C30, these registers are readable as RR9, RR4, RR5, and RR11, respectively, when WR7' D6=1. Refer to the description of WR7 Prime for enabling the extended read capability.
3. This feature is not available on NMOS.

Table 5-2. SCC Read Registers

Reg	Description
RR0	Transmit and Receive buffer status and external status
RR1	Special Receive Condition status
RR2	Modified interrupt vector (Channel B only), Unmodified interrupt vector (Channel A only)
RR3	Interrupt pending bits (Channel A only)
RR4 ²	Transmit and Receive modes and parameters (WR4)
RR5 ²	Transmit parameters and control modes (WR5)
RR6 ³	SDLC FIFO byte counter lower byte (only when enabled)
RR7 ³	SDLC FIFO byte count and status (only when enabled)
RR8	Receive buffer
RR9 ²	Receive parameters and control modes (WR3)
RR10	Miscellaneous status bits
RR11 ²	Miscellaneous transmit and receive control bits (WR10)
RR12	Lower byte of baud rate generator time constant
RR13	Upper byte of baud rate generator time constant
RR14 ²	Extended Feature and FIFO Control (WR7 Prime)
RR15	External Status interrupt information

5.1 INTRODUCTION (Continued)

Among these registers, WR9 (Master Interrupt Control and Reset register) can be accessed through either channel. The RR2 (Interrupt Vector register) returns the interrupt vector modified by status, if read from Channel B, and written value (without modification), if read from Channel A.

Channel A has an additional read register which contains all the Interrupt Pending bits (RR3A).

Write Registers. Eleven write registers are used for control (includes transmit buffer/FIFO); two for sync character generation/detection; two for baud rate generation. In addition, there are two write registers which are shared by both channels; one is the interrupt vector register (WR2); the other is the Master Interrupt and Reset register (WR9).

On the ESCC and 85C30, there is one additional register (WR7') to control enhanced features.

See Table 5-1 for a summary of Write registers.

Read Registers. Four read registers indicate status information; two are for baud rate generation; one for the receive buffer. In addition, there are two read registers which are shared by both channels; one for the interrupt pending bits; another for the interrupt vector. On the CMOS/ESCC, there are two additional registers, RR6 and RR7. They are available if the Frame Status FIFO feature was enabled in the SDLC mode of operation. On the ESCC, there is an "extended read" option and if its enabled, certain write registers can be read back.

See Table 5-2 for a summary of Read registers.

5.2 WRITE REGISTERS

The SCC write register set in each channel has 11 control registers (includes transmit buffer/FIFO), two sync character registers, and two baud rate time constant registers. The interrupt control register and the master interrupt control and reset register are shared by both channels. In addition to these, the ESCC and 85C30 has a register (WR7'; prime 7) to control the enhancements.

Between 80X30 and 85X30, the variation in register definition is a command decode structure; Write Register 0 (WR0). The following sections describe in detail each write register and the associated bit configuration for each.

The following sections describe WR registers in detail:

5.2.1 Write Register 0 (Command Register)

WR0 is the command register and the CRC reset code register. WR0 takes on slightly different forms depending upon whether the SCC is in the Z85X30 or the Z80X30. Figure 5-1 shows the bit configuration for the Z85X30 and includes register select bits in addition to command and reset codes.

Figure 5-2 shows the bit configuration for the Z80X30 and includes (in Channel B only) the address decoding select described later.

The following bit description for WR0 is identical for both versions except where specified:

Bits D7 and D6: CRC Reset Codes 1 And 0.

Null Command (00). This command has no effect on the SCC and is used when a write to WR0 is necessary for some reason other than a CRC Reset command.

Reset Receive CRC Checker Command (01). This command is used to initialize the receive CRC circuitry. It is necessary in synchronous modes (except SDLC) if the Enter Hunt Mode command in Write Register 3 is not issued between received messages. Any action that disables the receiver initializes the CRC circuitry. Resetting the Receive CRC Checker command is accomplished automatically in SDLC mode.

Reset Transmit CRC Generator Command (10). This command initializes the CRC generator. It is usually issued in the initialization routine and after the CRC has been transmitted. A Channel Reset does not initialize the generator and this command is not issued until after the transmitter has been enabled in the initialization routine.

On the ESCC and 85C30, this command is not needed if Auto EOM Reset mode is enabled (WR7' D1=1).

Reset Transmit Underrun/EOM Latch Command (11). This command controls the transmission of CRC at the end of transmission (EOM). If this latch has been reset, and a transmit underrun occurs, the SCC automatically appends CRC to the message. In SDLC mode with Abort on Underrun selected, the SCC sends an abort and Flag on underrun if the TX Underrun/EOM latch has been reset.

Write Register 0 (non-multiplexed bus mode)

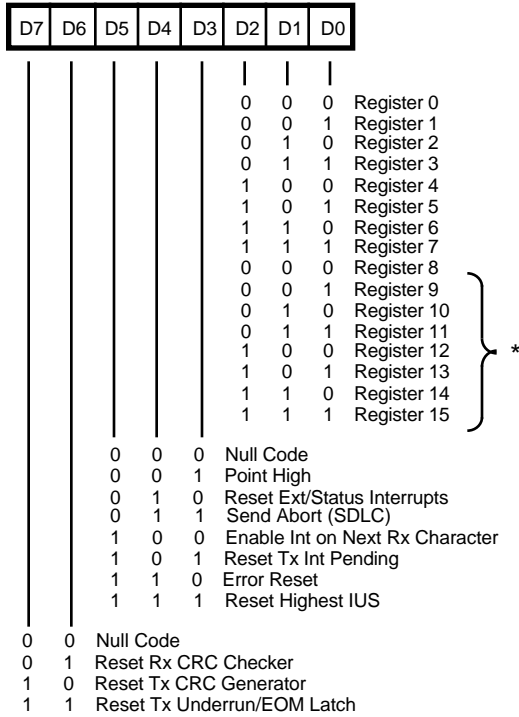


Figure 5-1. Write Register 0 in the Z85X30

Write Register 0 (multiplexed bus mode)

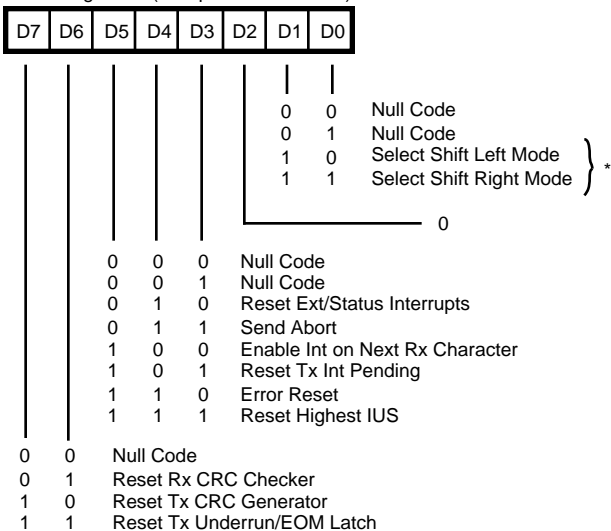


Figure 5-2. Write Register 0 in the Z80X30

At the start of the CRC transmission, the Tx Underrun/EOM latch is set. The Reset command can be issued at any time during a message. If the transmitter is disabled, this command does not reset the latch. However, if no External Status interrupt is pending, or if a Reset External Status interrupt command accompanies this command while the transmitter is disabled, an External/Status interrupt is generated with the Tx Underrun/EOM bit reset in RR0.

Bits D5-D3: Command Codes for the SCC.

Null Command (000). The Null command has no effect on the SCC.

Point High Command (001). This command effectively adds eight to the Register Pointer (D2-D0) by allowing WR8 through WR15 to be accessed. The Point High command and the Register Pointer bits are written simultaneously. This command is used in the Z85X30 version of the SCC. Note that WR0 changes form depending upon the SCC version. Register access for the Z80X30 version of the SCC is accomplished through direct addressing.

Reset External/Status Interrupts Command (010). After an External/Status interrupt (a change on a modem line or a break condition, for example), the status bits in RR0 are latched. This command re-enables the bits and allows interrupts to occur again as a result of a status change. Latching the status bits captures short pulses until the CPU has time to read the change.

The SCC contains simple queueing logic associated with most of the external status bits in RR0. If another External/Status condition changes while a previous condition is still pending (Reset External/Status Interrupt has not yet been issued) and this condition persists until after the command is issued, this second change causes another External/Status interrupt. However, if this second status change does not persist (there are two transitions), another interrupt is not generated. Exceptions to this rule are detailed in the RR0 description.

Send Abort Command (011). This command is used in SDLC mode to transmit a sequence of eight to thirteen 1s. This command always empties the transmit buffer and sets Tx Underrun/EOM bit in Read Register 0.

Enable Interrupt On Next Rx Character Command (100). If the interrupt on First Received Character mode is selected, this command is used to reactivate that mode after each message is received. The next character to enter the Receive FIFO causes a Receive interrupt. Alternatively, the first previously stored character in the FIFO causes a Receive interrupt.

5.1 INTRODUCTION (Continued)

Reset Tx Interrupt Pending Command (101). This command is used in cases where there are no more characters to be sent; e.g., at the end of a message. This command prevents further transmit interrupts until after the next character has been loaded into the transmit buffer or until CRC has been completely sent. This command is necessary to prevent the transmitter from requesting an interrupt when the transmit buffer becomes empty (with Transmit Interrupt Enabled).

Error Reset Command (110). This command resets the error bits in RR1. If interrupt on first Rx Character or Interrupt on Special Condition modes is selected and a special condition exists, the data with the special condition is held in the Receive FIFO until this command is issued. If either of these modes is selected and this command is issued before the data has been read from the Receive FIFO, the data is lost.

Reset Highest IUS Command (110). This command resets the highest priority Interrupt Under Service (IUS) bit, allowing lower priority conditions to request interrupts. This command allows the use of the internal daisy chain (even in systems without an external daisy chain) and is the last operation in an interrupt service routine.

Bits 2 through 0: Register Selection Code

On the Z85X30, these three bits select Registers 0 through 7. With the Point High command, Registers 8 through 15 are selected (Table 5-3).

In the multiplexed bus mode, bits D2 through D0 have the following function.

Bit D2 must be programmed as 0. Bits D1 and D0 select Shift Left/Right; that is WR0 (1-0)=10 for shift left and WR0 (1-0)=11 for shift right. See Section 2.1.4 for further details on Z80X30 register access.

5.2.2 Write Register 1 (Transmit/Receive Interrupt and Data Transfer Mode Definition)

Write Register 1 is the control register for the various SCC interrupt and Wait/Request modes. Figure 5-3 shows the bit assignments for WR1.

Bit 7: WAIT/DMA Request Enable.

This bit enables the Wait/Request function in conjunction with the Request/Wait Function Select bit (D6).

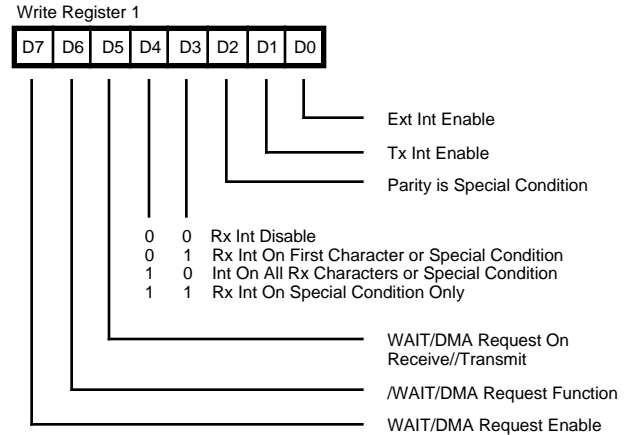


Figure 5-3. Write Register 1

When programmed to 0, the selected function (bit 6) forces the /W//REQ pin into the appropriate inactive state (High for Request, floating for Wait).

When programmed to 1, the state of bit 6 determines the activity of the /W//REQ pin (Wait or Request).

Bit 6: WAIT/DMA Request Function

When programmed to 0, the Wait function is selected. In the Wait mode, the /W//REQ pin switches from floating to Low when the CPU attempts to transfer data before the SCC is ready.

When programmed to 1, the Request function is selected. In the Request mode, the /W//REQ pin switches from High to Low when the SCC is ready to transfer data.

Bit 5: /WAIT//REQUEST on Transmit or Receive

When programmed to 0, the state of the /W//REQ pin is determined by bit 6 and the state of the transmit buffer.

Note: A transmit request function is available on the /DTR//REQ pin. This allows full-duplex operation under DMA control for both channels.

Table 5-3. Z85X30 Register Map

A/B	PNT2	PNT1	PNT0	WRITE	READ 8530 85C30/230* WR15 D2 = 0	85C30/230 WR15 D2=1	85C30/85230W R15 D2=1 WR7' D6=1
0	0	0	0	WR0B	RR0B	RR0B	RR0B
0	0	0	1	WR1B	RR1B	RR1B	RR1B
0	0	1	0	WR2	RR2B	RR2B	RR2B
0	0	1	1	WR3B	RR3B	RR3B	RR3B
0	1	0	0	WR4B	(RR0B)	(RR0B)	(WR4B)
0	1	0	1	WR5B	(RR1B)	(RR1B)	(WR5B)
0	1	1	0	WR6B	(RR2B)	RR6B	RR6B
0	1	1	1	WR7B	(RR3B)	RR7B	RR7B
1	0	0	0	WR0A	RR0A	RR0A	RR0A
1	0	0	1	WR1A	RR1A	RR1A	RR1A
1	0	1	0	WR2	RR2A	RR2A	RR2A
1	0	1	1	WR3A	RR3A	RR3A	RR3A
1	1	0	0	WR4A	(RR0A)	(RR0A)	(WR4A)
1	1	0	1	WR5A	(RR1A)	(RR1A)	(WR5A)
1	1	1	0	WR6A	(RR2A)	RR6A	RR6A
1	1	1	1	WR7A	(RR3A)	RR7A	RR7A

With Point High Command

0	0	0	0	WR8B	RR8B	RR8B	RR8B
0	0	0	1	WR9	(RR13B)	(RR13B)	(WR3B)
0	0	1	0	WR10B	RR10B	RR10B	RR10B
0	0	1	1	WR11B	(RR15B)	(RR15B)	(WR10B)
0	1	0	0	WR12B	RR12B	RR12B	RR12B
0	1	0	1	WR13B	RR13B	RR13B	RR13B
0	1	1	0	WR14B	RR14B	RR14B	(WR7'B)
0	1	1	1	WR15B	RR15B	RR15B	RR15B
1	0	0	0	WR8A	RR8A	RR8A	RR8A
1	0	0	1	WR9A	(RR13A)	(RR13A)	(WR3A)
1	0	1	0	WR10A	RR10A	RR10A	RR10A
1	0	1	1	WR11A	(RR15A)	(RR15A)	(WR10A)
1	1	0	0	WR12A	RR12A	RR12A	RR12A
1	1	0	1	WR13A	RR13A	RR13A	RR13A
1	1	1	0	WR14A	RR14A	RR14A	(WR7'A)
1	1	1	1	WR15A	RR15A	RR15A	RR15A

Notes:

WR15 bit D2 enables status FIFO function. (Not available on NMOS)

WR7' bit D6 enables extend read function. (Only on ESCC and 85C30)

* Includes 85C30 and 85230 with WR15 D2=0.

5.1 INTRODUCTION (Continued)

When programmed to 1, this bit allows the Wait/Request function to follow the state of the receive buffer. Thus, depending on the state of bit 6, the /W//REQ pin is active or inactive in relation to the empty or full state of the receive buffer.

The request function occurs only when the SCC is not selected; e.g., if the internal request becomes active while the SCC is in the middle of a read or write cycle, the external request does not become active until the cycle is complete. An active request output causes a DMA controller to initiate a read or write operation. If the request on Transmit mode is selected in either SDLC or Synchronous Mode, the Request pin is pulsed Low for one PCLK cycle at the end of CRC transmission to allow the immediate transmission of another block of data.

In the Wait On Receive mode, the /WAIT pin is active if the CPU attempts to read SCC data that has not yet been received. In the Wait On Transmit mode, the /WAIT pin is active if the CPU attempts to write data when the transmit buffer is still full. Both situations occur frequently when block transfer instructions are used.

Bits 4 and 3: Receive Interrupt Modes

Receive Interrupts Disabled (00). This mode prevents the receiver from requesting an interrupt. It is normally used in a polled environment where either the status bits in RR0 or the modified vector in RR2 (Channel B) are monitored to initiate a service routine. Although the receiver interrupts are disabled, a special condition can still provide a unique vector status in RR2.

Receive Interrupt on First Character or Special Condition (01). The receiver requests an interrupt in this mode on the first available character (or stored FIFO character) or on a special condition. Sync characters, stripped from the message stream, do not cause interrupts.

Special receive conditions are: receiver overrun, framing error, end of frame, or parity error (if selected). If a special receive condition occurs, the data containing the error is stored in the Receive FIFO until an Error Reset command is issued by the CPU.

This mode is usually selected when a Block Transfer mode is used. In this interrupt mode, a pending special receive condition remains set until either an error Reset command, a channel or hardware reset, or until receive interrupts are disabled.

The Receive Interrupt on First Character or Special Condition mode can be re-enabled by the Enable Rx Interrupt on Next Character command in WR0.

ESCC:

See the description of WR7' on how this function can be changed.

Interrupt on All Receive Characters or Special Condition (10). This mode allows an interrupt for every character received (or character in the Receive FIFO) and provides a unique vector when a special condition exists. The Receiver Overrun bit and the Parity Error bit in RR1 are two special conditions that are latched. These two bits are reset by the Error Reset command. Receiver overrun is always a special receive condition, and parity can be programmed to be a special condition.

Data characters with special receive conditions are not held in the Receive FIFO in the Interrupt On All Receive Characters or Special Conditions Mode as they are in the other receive interrupt modes.

Receive Interrupt on Special Condition (11). This mode allows the receiver to interrupt only on characters with a special receive condition. When an interrupt occurs, the data containing the error is held in the Receive FIFO until an Error Reset command is issued. When using this mode in conjunction with a DMA, the DMA is initialized and enabled before any characters have been received by the ESCC. This eliminates the time-critical section of code required in the Receive Interrupt on First Character or Special Condition mode. Hence, all data can be transferred via the DMA so that the CPU need not handle the first received character as a special case. In SDLC mode, if the SDLC Frame Status FIFO is enabled and an EOF is received, an interrupt with vector for receive data available is generated and the Receive FIFO is not locked.

Bit 2: Parity Is Special Condition

If this bit is set to 1, any received characters with parity not matching the sense programmed in WR4 give rise to a Special Receive Condition. If parity is disabled (WR4), this bit is ignored. A special condition modifies the status of the interrupt vector stored in WR2. During an interrupt acknowledgment cycle, this vector can be placed on the data bus.

Bit 1: Transmitter Interrupt Enable

If this bit is set to 1, the transmitter requests an interrupt whenever the transmit buffer becomes empty.

Bit 0: External/Status Master Interrupt Enable

This bit is the master enable for External/Status interrupts including /DCD, /CTS, /SYNC pins, break, abort, the beginning of CRC transmission when the Transmit/Under-run/EOM latch is set, or when the counter in the baud rate generator reaches 0. Write Register 15 contains the individual enable bits for each of these sources of External/Status interrupts. This bit is reset by a channel or hardware reset.

5.2.3 Write Register 2 (Interrupt Vector)

WR2 is the interrupt vector register. Only one vector register exists in the SCC, and it can be accessed through either channel. The interrupt vector can be modified by status information. This is controlled by the Vector Includes Status (VIS) and the Status High/Status Low bits in WR9. The bit positions for WR2 are shown in Figure 5-4.

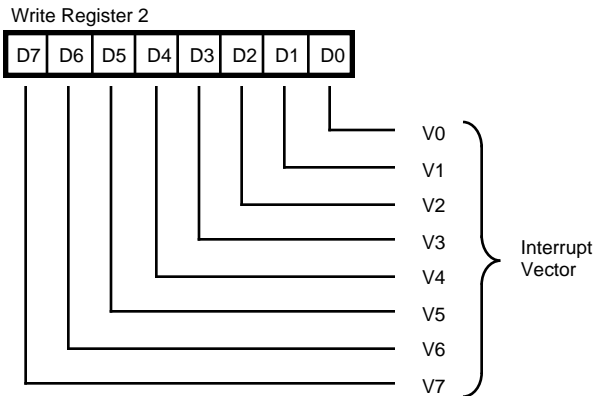


Figure 5-4. Write Register 2

5.2.4 Write Register 3 (Receive Parameters and Control)

This register contains the control bits and parameters for the receiver logic as illustrated in Figure 5-5. On the ESCC and 85C30, with the Extended Read option enabled, this register may be read as RR9.

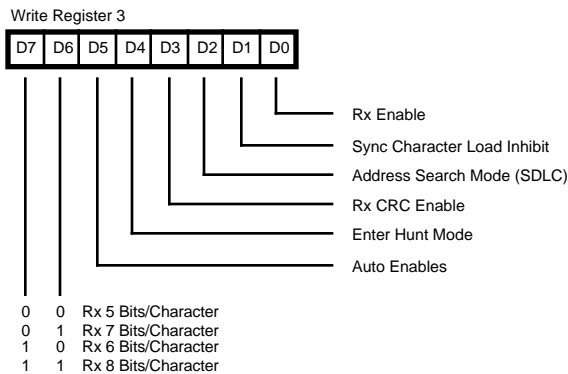


Figure 5-5. Write Register 3

Bits 7 and 6: Receiver Bits/Character

The state of these two bits determines the number of bits to be assembled as a character in the received serial data stream. The number of bits per character can be changed while a character is being assembled, but only before the number of bits currently programmed is reached. Unused bits in the Received Data Register (RR8) are set to 1 in asynchronous modes. In Synchronous and SDLC modes, the SCC merely transfers an 8-bit section of the serial data stream to the Receive FIFO at the appropriate time. Table 5-4 lists the number of bits per character in the assembled character format.

Table 5-4. Receive Bits per Character

D7	D6	Bits/Character
0	0	5
0	1	7
1	0	6
1	1	8

Bit 5: Auto Enable

This bit programs the function for both the /DCD and /CTS pins. /CTS becomes the transmitter enable and /DCD becomes the receiver enable when this bit is set to 1. However, the Receiver Enable and Transmit Enable bits must be set before the /DCD and /CTS pins can be used in this manner. When the Auto Enable bit is set to 0, the /DCD and /CTS pins are inputs to the corresponding status bits in Read Register 0. The state of /DCD is ignored in the Local Loopback mode. The state of /CTS is ignored in both Auto Echo and Local Loopback modes.

Bit 4: Enter Hunt Mode

This command forces the comparison of sync characters or flags to assembled receive characters for the purpose of synchronization. After reset, the SCC automatically enters the Hunt mode (except asynchronous). Whenever a flag or sync character is matched, the Sync/Hunt bit in Read Register 0 is reset and, if External/Status Interrupt Enable is set, an interrupt sequence is initiated. The SCC automatically enters the Hunt mode when an abort condition is received or when the receiver is enabled.

Bit 3: Receiver CRC Enable

This bit is used to initiate CRC calculation at the beginning of the last byte transferred from the Receiver Shift register to the Receive FIFO. This operation occurs independently of the number of bytes in the Receive FIFO. When a particular byte is to be excluded from the CRC calculation, this bit should be reset before the next byte is transferred to the Receive FIFO. If this feature is used, care must be taken to ensure that eight bits per character is selected in the receiver because of an inherent delay from the Receive Shift register to the CRC checker.

5.1 INTRODUCTION (Continued)

This bit is internally set to 1 in SDLC mode and the SCC calculates the CRC on all bits except zeros inserted between the opening and closing flags. This bit is ignored in asynchronous modes.

Bit 2: Address Search Mode (SDLC)

Setting this bit in SDLC mode causes messages with addresses not matching the address programmed in WR6 to be rejected. No receiver interrupts occur in this mode unless there is an address match. The address that the SCC attempts to match is unique (1 in 256) or multiple (16 in 256), depending on the state of Sync Character Load Inhibit bit. Address FFH is always recognized as a global address. The Address Search mode bit is ignored in all modes except SDLC.

Bit 1: SYNC Character Load Inhibit

If this bit is set to 1 in any mode except SDLC, the SCC compares the byte in WR6 with the byte about to be stored in the FIFO, and it inhibits this load if the bytes are equal. (Caution: this also occurs in the asynchronous mode if the received character matches the contents of WR6.) The SCC does not calculate the CRC on bytes stripped from the data stream in this manner. If the 6-bit sync option is selected while in Monosync mode, the comparison is still across eight bits, so WR6 is programmed for proper operation.

If the 6-bit sync option is selected with this bit set to 1, all sync characters except the one immediately preceding the data are stripped from the message. If the 6-bit sync option is selected while in the Bisync mode, this bit is ignored.

The address recognition logic of the receiver is modified in SDLC mode if this bit is set to 1, i.e., only the four most significant bits of WR6 must match the receiver address. This procedure allows the SCC to receive frames from up to 16 separate sources without programming WR6 for each source (if each station address has the four most significant bits in common). The address field in the frame is still eight bits long. Address FFH is always recognized as a global address.

The bit is ignored in SDLC mode if Address Search mode has not been selected.

Bit 0: Receiver Enable

When this bit is set to 1, receiver operation begins. This bit should be set only after all other receiver parameters are established and the receiver is completely initialized. This bit is reset by a channel or hardware reset command, and it disables the receiver.

5.2.5 Write Register 4 (Transmit/Receive Miscellaneous Parameters and Modes)

WR4 contains the control bits for both the receiver and the transmitter. These bits should be set in the transmit and receiver initialization routine before issuing the contents of WR1, WR3, WR6, and WR7. Bit positions for WR4 are shown in Figure 5-6. On the ESCC and 85C30, with the Extended Read option enabled, this register is read as RR4.

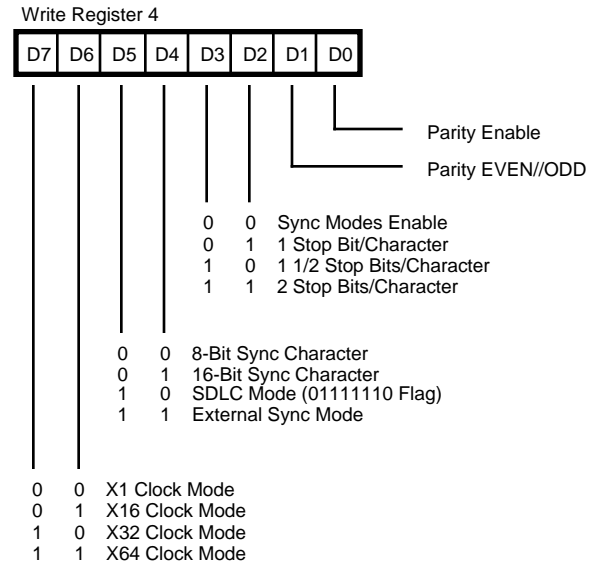


Figure 5-6. Write Register 4

Bits 7 and 6: Clock Rate bits 1 and 0

These bits specify the multiplier between the clock and data rates. In synchronous modes, the 1X mode is forced internally and these bits are ignored unless External Sync mode has been selected.

1X Mode (00). The clock rate and data rate are the same. In External Sync mode, this bit combination specifies that only the /SYNC pin is used to achieve character synchronization.

16X Mode (01). The clock rate is 16 times the data rate. In External Sync mode, this bit combination specifies that only the /SYNC pin is used to achieve character synchronization.

32X Mode (10). The clock rate is 32 times the data rate. In External Sync mode, this bit combination specifies that either the /SYNC pin or a match with the character stored in WR7 will signal character synchronization. The sync character can be either six or eight bits long as specified by the 6-bit/8-bit sync bit in WR10.

64X Mode (11). The clock rate is 64 times the data rate. With this bit combination in External Sync mode, both the receiver and transmitter are placed in SDLC mode. The only variation from normal SDLC operation is that the /SYNC pin is used to start or stop the reception of a frame by forcing the receiver to act as though a flag had been received.

Bits 5 and 4: SYNC Mode selection bits 1 and 0

These two bits select the various options for character synchronization. They are ignored unless synchronous modes are selected in the stop bits field of this register.

Monosync Mode (00). In this mode, the receiver achieves character synchronization by matching the character stored in WR7 with an identical character in the received data stream. The transmitter uses the character stored in WR6 as a time fill. The sync character is either six or eight bits, depending on the state of the 6-bit/8-bit sync bit in WR10. If the Sync Character Load Inhibit bit is set, the receiver strips the contents of WR6 from the data stream if received within character boundaries.

Bisync Mode (01). The concatenation of WR7 with WR6 is used for receiver synchronization and as a time fill by the transmitter. The sync character is 12 or 16 bits in the receiver, depending on the state of the 6-bit/8-bit sync bit in WR10. The transmitted character is always 16 bits.

SDLC Mode (10). In this mode, SDLC is selected and requires a Flag (01111110) to be written to WR7. The receiver address field is written to WR6. The SDLC CRC polynomial is also selected (WR5) in SDLC mode.

External Sync Mode (11). In this mode, the SCC expects external logic to signal character synchronization via the /SYNC pin. If the crystal oscillator option is selected (in WR11), the internal /SYNC signal is forced to 0. In this mode, the transmitter is in Monosync mode using the contents of WR6 as the time fill with the sync character length specified by the 6-bit/8-bit Sync bit in WR10.

Bits 3 and 2: Stop Bits selection, bits 1 and 0

These bits determine the number of stop bits added to each asynchronous character that is transmitted. The receiver always checks for one stop bit in Asynchronous mode. A special mode specifies that a Synchronous mode is to be selected. D2 is always set to 1 by a channel or hardware reset to ensure that the /SYNC pin is in a known state after a reset.

Synchronous Modes Enable (00). This bit combination selects one of the synchronous modes specified by bits D4, D5, D6, and D7 of this register and forces the 1X Clock mode internally.

1 Stop Bit/Character (01). This bit selects Asynchronous mode with one stop bit per character.

1 1/2 Stop Bits/Character (10). These bits select Asynchronous mode with 1-1/2 stop bits per character. This mode is not used with the 1X clock mode.

2 Stop Bits/Character (11). These bits select Asynchronous mode with two stop bits per transmitted character and checks for one received stop bit.

Bit 1: Parity Even/Odd select bit

This bit determines whether parity is checked as even or odd. A 1 programmed here selects even parity, and a 0 selects odd parity. This bit is ignored if the Parity enable bit is not set.

Bit 0: Parity Enable

When this bit is set, an additional bit position beyond those specified in the bits/character control is added to the transmitted data and is expected in the receive data. The Received Parity bit is transferred to the CPU as part of the data unless eight bits per character is selected in the receiver.

5.2.6 Write Register 5 (Transmit Parameters and Controls)

WR5 contains control bits that affect the operation of the transmitter. D2 affects both the transmitter and the receiver. Bit positions for WR5 are shown in Figure 5-7. On the 85X30 with the Extended Read option enabled, this register is read as RR5.

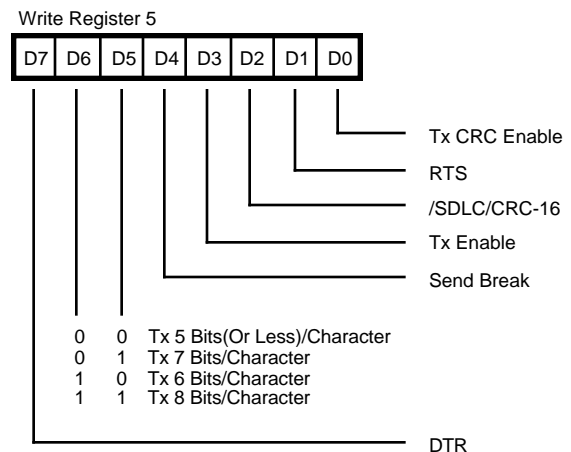


Figure 5-7. Write Register 5

Bit 7: Data Terminal Ready control bit

This is the control bit for the /DTR//REQ pin while the pin is in the DTR mode (selected in WR14). When set, /DTR is Low; when reset, /DTR is High. This bit is ignored when /DTR//REQ is programmed to act as a /REQ pin. This bit is reset by a channel or hardware reset.

5.1 INTRODUCTION (Continued)

Bits 6 and 5: Transmit Bits/Character select bits 1 and 0

These bits control the number of bits in each byte transferred to the transmit buffer. Bits sent must be right justified with the least significant bits first.

The Five Or Less mode allows transmission of one to five bits per character. For five or fewer bits per character, the data character must be formatted as shown below in Table 5-5. In the Six or Seven Bits/Character modes, unused data bits are ignored.

Bit 4: Send Break control bit

When set, this bit forces the TxD output to send continuous 0s beginning with the following transmit clock, regardless of any data being transmitted at the time. This bit functions whether or not the transmitter is enabled. When reset, TxD continues to send the contents of the Transmit Shift register, which might be syncs, data, or all 1s. If this bit is set while in the X21 mode (Monosync and Loop mode selected) and character synchronization is achieved in the receiver, this bit is automatically reset and the transmitter begins sending syncs or data. This bit is also reset by a channel or hardware reset.

Table 5-5. Transmit Bits per Character

Bit 7	Bit 6	
0	0	5 or less bits/character
0	1	7 bits/character
1	0	6 bits/character
1	1	8 bits/character

Note: For five or less bits per character selection in WR5, the following encoding is used in the data sent to the transmitter. D is the data bit(s) to be sent.

D7	D6	D5	D4	D3	D2	D1	D0	
1	1	1	1	0	0	0	D	Sends one data bit
1	1	1	0	0	0	D	D	Sends two data bits
1	1	0	0	0	D	D	D	Sends three data bits
1	0	0	0	D	D	D	D	Sends four data bits
0	0	0	D	D	D	D	D	Sends five data bits

Bit 3: Transmit Enable

Data is not transmitted until this bit is set, and the TxD output sends continuous 1s unless Auto Echo mode or SDLC Loop mode is selected. If this bit is reset after transmission starts, the transmission of data or sync characters is completed. If the transmitter is disabled during the transmission of a CRC character, sync or flag characters are sent instead of CRC. This bit is reset by a channel or hardware reset.

Bit 2: SDLC/CRC-16 polynomial select bit

This bit selects the CRC polynomial used by both the transmitter and receiver. When set, the CRC-16 polynomial is used; when reset, the SDLC polynomial is used. The SDLC/CRC polynomial is selected when SDLC mode is selected. The CRC generator and checker can be preset to all 0s or all 1s, depending on the state of the Preset 1/Preset 0 bit in WR10.

Bit 1: Request To Send control bit

This is the control bit for the /RTS pin. When the RTS bit is set, the /RTS pin goes Low; when reset, /RTS goes High. When Auto Enable is set in asynchronous mode, the /RTS pin immediately goes Low when the RTS bit is set. However, when the RTS bit is reset, the /RTS pin remains Low until the transmitter is completely empty and the last stop bit has left the TxD pin. In synchronous modes, the /RTS pin directly follows the state of this bit, except in SDLC mode under specific conditions. In SDLC mode, if Flag On Underrun bit (WR10, D2) is set, RTS bit in WR5 is reset, and D2 in WR7' is set. The /RTS pin deasserts automatically at the last bit of the closing flag triggered by the rising edge of the Tx clock. This bit is reset by a channel or hardware reset.

Bit 0: Transmit CRC Enable

This bit determines whether or not the CRC is calculated on a transmit character. If this bit is set at the time the character is loaded from the transmit buffer to the Transmit Shift register, the CRC is calculated on that character. The CRC is not automatically sent unless this bit is set when the transmit underrun exists.

5.2.7 Write Register 6 (Sync Characters or SDLC Address Field)

WR6 is programmed to contain the transmit sync character in the Monosync mode, or the first byte of a 16-bit sync character in the External Sync mode. WR6 is not used in asynchronous modes. In the SDLC modes, it is programmed to contain the secondary address field used to compare against the address field of the SDLC Frame. In SDLC mode, the SCC does not automatically transmit the station address at the beginning of a response frame. Bit positions for WR6 are shown in Figure 5-8.

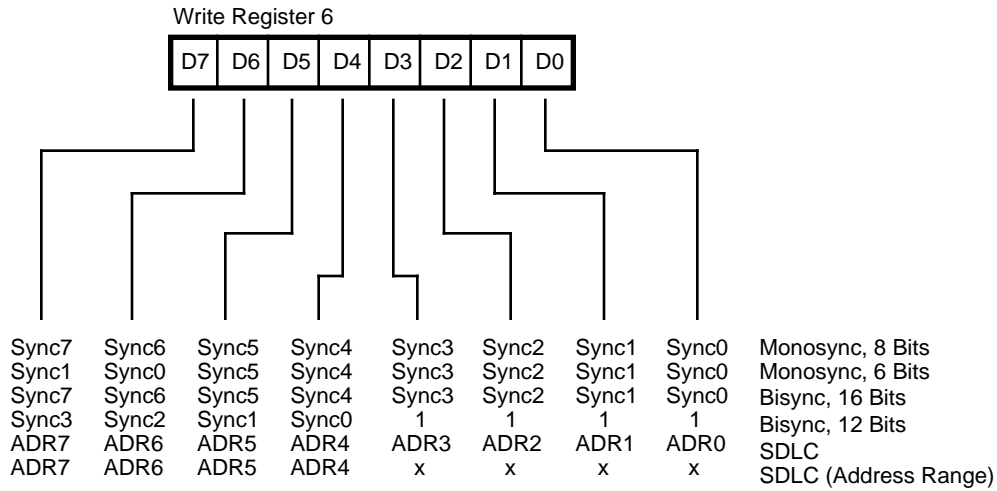


Figure 5-8. Write Register 6

5.2.8 Write Register 7 (Sync Character or SDLC Flag)

WR7 is programmed to contain the receive sync character in the Monosync mode, a second byte (the last eight bits) of a 16-bit sync character in the Bisync mode, or a Flag

character (01111110) in the SDLC modes. WR7 holds the receive sync character or a flag if one of the special versions of the External Sync mode is selected. WR7 is not used in Asynchronous mode. Bit positions for WR7 are shown in Figure 5-9.

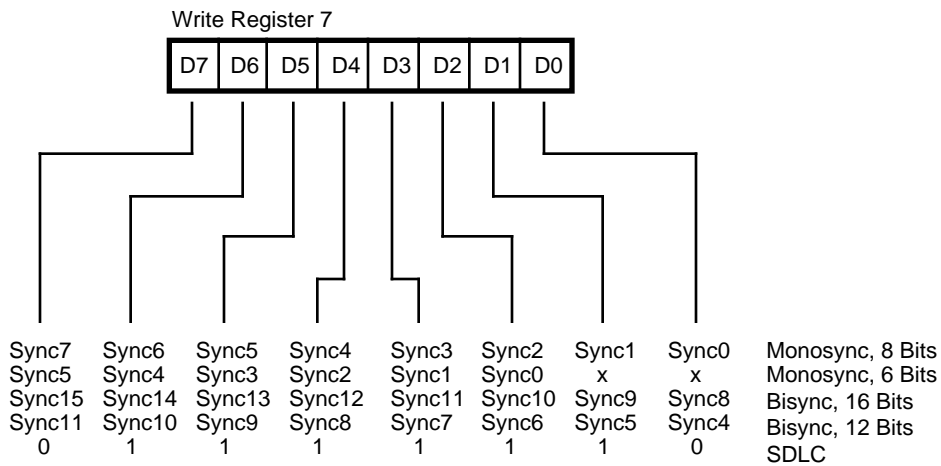


Figure 5-9. Write Register 7

5.1 INTRODUCTION (Continued)

5.2.9 Write Register 7 Prime (ESCC only)

This Register is used only with the ESCC. Write Register 7 Prime is located at the same address as Write Register 7. This register is written to by setting bit D0 of WR15 to a 1. Refer to the description in the section on Write Register 15. Features enabled in WR7 Prime remain enabled unless otherwise disabled; a hardware or channel reset leaves WR7 Prime with all features intact (register contents are 0) (Figure 5-10).

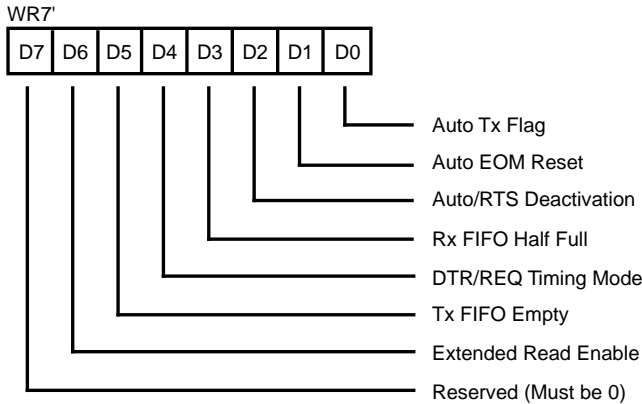


Figure 5-10. Write Register 7 Prime

Bit 7: Reserved

This bit is not used and must always be written zero.

Bit 6: Extended Read Enable bit

Setting this bit enables the reading of WR3, WR4, WR5, WR7 Prime and WR10. When this feature is enabled, these registers can be accessed by reading RR9, RR4, RR5, RR14, and RR11, respectively. When the extended read is not enabled, register access is identical to that of the NMOS/CMOS version. Refer to Chapter Two on how this feature affects the mapping of read registers.

Bit 5: Transmit FIFO Interrupt Level

If this bit is set, the transmit buffer empty interrupt is generated when the Transmit FIFO is completely empty. If this bit is reset (0), the transmit buffer empty interrupt is generated when the entry location of the Transmit FIFO is empty. This latter operation is identical to that of the NMOS/CMOS version.

In the DMA Request on Transmit Mode, when using either the /W//REQ or /DTR//REQ pins, the request is asserted when the Transmit FIFO is completely empty if the Transmit FIFO Interrupt Level bit is set. The request is asserted when the entry location of the Transmit FIFO is empty if the Transmit FIFO Interrupt Level bit is reset (0).

Bit 4: /DTR//REQ Timing

If this bit is set and the /DTR//REQ pin is used for Request Mode (WR14 bit D2 = 1), the deactivation of the /DTR//REQ pin is identical to the /W//REQ pin. Refer to the chapter on interfacing for further details. If this bit is reset (0), the deactivation time for the /DTR//REQ pin is 4TcPc. This latter operation is identical to that of the SCC.

Bit 3: Receive FIFO Interrupt Level

If WR7' D3=1 and "Receive Interrupt on All Characters and Special Conditions" is enabled, the Receive Character Available interrupt is triggered when the Rx FIFO is half full, i.e., the four byte slots of the Rx FIFO are empty. However, if any character has a special condition, a special condition interrupt is generated when the character is loaded into the Receive FIFO. Therefore, the special condition interrupt service routine should read RR1 before reading the data to determine which byte has which special condition.

If WR7' D3=0, the ESCC sets the receiver and generates the receive character available interrupt on every received character, regardless of any special receive condition.

Bit 2: Auto /RTS pin Deactivation

This bit controls the timing of the deassertion of the /RTS pin. If the ESCC is programmed for SDLC mode and Flag-On-Underrun (WR10 D2=0), this bit is set and the RTS bit is reset. The /RTS is deasserted automatically at the last bit of the closing flag, triggered by the rising edge of the Transmit Clock. If this bit is reset, the /RTS pin follows the state programmed in WR5 D1.

Bit 1: Automatic EOM Reset

If this bit is set, the ESCC automatically resets the Tx Underrun/EOM latch and presets the transmit CRC generator to its programmed preset state (per values set in WR5 D2 & WR10 D7). Therefore, it is not necessary to issue the Reset Tx Underrun/EOM latch command when this feature is enabled. If this bit is reset, ESCC operation is identical to the SCC.

Bit 0: Automatic Tx SDLC Flag

If this bit is set, the ESCC automatically transmits an SDLC flag before transmitting data. This removes the requirement to reset the mark idle bit (WR10 D3) before writing data to the transmitter, or having to enable the transmitter before writing data to the Transmit FIFO. Also, this feature enables a transmit data write before enabling the transmitter. If this bit is reset, operation is identical to that of the SCC.

5.2.10 Write Register 7 Prime (85C30 only)

This Register is used only with the CMOS 85C30 SCC. WR7' is written to by first setting bit D0 of WR15 to 1, and pointing to WR7 as normal. All writes to register 7 will be to WR7' so long as WR D0 is set. WR 15 bit D0 must be reset to 0 to address the sync register, WR7. If bit D6 of WR7' was set during the write, then WR7' can be read by accessing to RR14. The features remain enabled until specifically disabled, or disabled by a hardware or software reset. Figure 5-10a. shows WR7'.

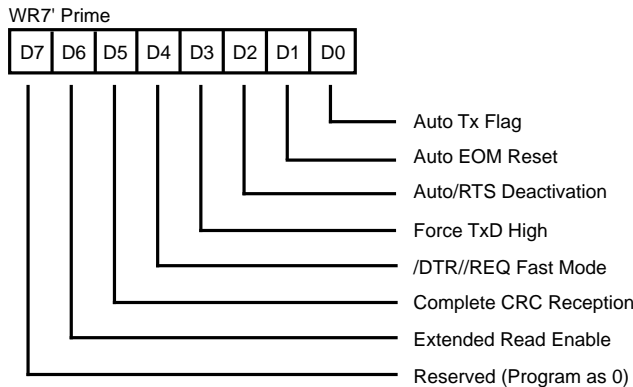


Figure 5-10a. Write Register 7 Prime (WR7')

Bit 7: Reserved.

This bit is reserved and must be programmed as 0.

Bit 6: Extended Read Enable bit

This bit enables the Extended Read. Setting this bit enables the reading of WR3, WR4, WR5, WR7' and WR10. When this feature is enabled, these registers can be accessed by reading RR9, RR4, RR5, RR14, and RR11, respectively. When this feature is not enabled, register access is to the SCC. In this case, read to these register locations returns RR13, RR0, RR1, RR10, and RR15 respectively.

Bit 5: Receive Complete CRC

On this version, with this bit set to 1, the 2nd byte of the CRC is received completely. This feature is ideal for applications which require a 2nd CRC byte for complete data; for example, a protocol analyzer or applications using other than CRC-CCITT CRC (i.e., 32bit CRC).

In SDLC mode of operation, the CMOS SCC, on this bit is programmed as 0. In this case on the EOF condition (when the closing flag is detected), the contents of the Receive Shift Register are transferred to the Receive Data FIFO regardless of the number of bits assembled. Because of the three-bit delay path between the sync register and the Receive Shift register, the last two bits of the 2nd byte of the CRC are never transferred to the Receive Data FIFO. The

data is actually formed with the six Least Significant Bits of the 2nd CRC byte.

Bit 4: /DTR//REQ Timing Fast Mode.

If this bit is set and the /DTR//REQ pin is used for Request Mode (WR14, bit D2=1), the deactivation of the /DTR//REQ pin is identical to the /W//REQ pin, which is triggered on the falling edge of the /WR signal, and the /DTR//REQ pin goes inactive below 200 ns (this number varies depending on the speed grade of the device). When this bit is reset to 0, the deactivation time for the /DTR//REQ pin is 4TcPc.

Bit 3: Force TxD High.

In the SDLC mode of operation with the NRZI encoding mode, there is an option to force TxD High. If bit D0 of WR15 is set to 1, bit D3 of WR7' can be used to set TxD pin High.

Note that the operation of this bit is independent of the Tx Enable bit in WR5 is used to control transmission activities, whereas bit D3 of WR7' acts as a pseudo transmitter may actually be mark or flag idling. Care must be exercised when setting this bit because any character being transmitted at the time that bit is set is "chopped off"; data written to the Transmit Buffer while this bit is set is lost.

Bit 2: Auto /RTS pin Deactivation

This bit controls the timing of the deassertion of the /RTS pin. If this device is programmed for SDLC mode and Flag-On-Underrun (WR10 D2=0), this bit is set and the RTS bit is reset. The /RTS is deasserted automatically at the last bit of the closing flag, triggered by the rising edge of the TxC. If this bit is reset to 0, the /RTS pin follows the state programmed in WR5 bit D1.

Bit 1: Automatic Tx Underrun/EOM Latch Reset

If this bit is set, this version automatically resets the Tx Underrun/EOM latch and presets the transmit CRC generator to its programmed preset state (the values set in WR5 D2 & WR10 D7). This removes the requirement to issue the Reset Tx Underrun/EOM latch command. Also, this feature enables a write transmit data before enabling the transmitter.

Bit 0: Automatic SDLC Opening Flag Transmission.

If this bit is set, the device automatically transmits an SDLC opening flag before transmitting data. This removes the requirement to reset the mark idle bit (WR10, bit D3) before writing data to the transmitter, or having to enable the transmitter before writing data to the Transmit buffer. Also, this feature enables a write transmit data before enabling the transmitter.

5.2.11 Write Register 8 (Transmit Buffer)

WR8 is the transmit buffer register.

5.1 INTRODUCTION (Continued)

5.2.12 Write Register 9 (Master Interrupt Control)

WR9 is the Master Interrupt Control register and contains the Reset command bits. Only one WR9 exists in the SCC and is accessed from either channel. The Interrupt control bits are programmed at the same time as the Reset command, because these bits are only reset by a hardware reset. Bit positions for WR9 are shown in Figure 5-11.

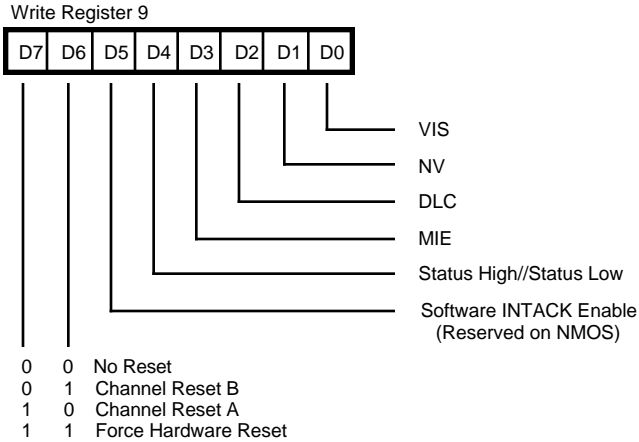


Figure 5-11. Write Register 9

Bit 7 and 6: Reset Command Bits

Together, these bits select one of the reset commands for the SCC. Setting either of these bits to 1 disables both the receiver and the transmitter in the corresponding channel; forces TxD for that channel marking, forces the modem control signals High in that channel, resets all IPs and IUSs and disables all interrupts in that channel. Four extra PCLK cycles must be allowed beyond the usual cycle time after any of the reset commands is issued before any additional commands or controls are written to the channel affected.

Null Command (00). This command has no effect. It is used when a write to WR9 is necessary for some reason other than an SCC Reset command.

Channel Reset B Command (01). Issuing this command causes a channel reset to be performed on Channel B.

Channel Reset A Command (10). Issuing this command causes a channel reset to be performed on Channel A.

Force Hardware Reset Command (11). The effects of this command are identical to those of a hardware reset, except that the Shift Right/Shift Left bit is not changed and the MIE, Status High/Status Low and DLC bits take the programmed values that accompany this command.

Bit 5: Software Interrupt Acknowledge control bit

If bit D5 is set, reading Read Register 2 (RR2) results in an interrupt acknowledge cycle to be executed internally. Like a hardware INTACK cycle, a software acknowledge causes the INT pin to return High, the IEO pin to go Low, and sets the IUS latch for the highest priority interrupt pending.

This bit is reserved on NMOS, and always writes as 0.

Bit 4: Status High/Status Low control bit

This bit controls which vector bits the SCC modifies to indicate status. When set to 1, the SCC modifies bits V6, V5, and V4 according to Table 5-6. When set to 0, the SCC modifies bits V1, V2, and V3. This bit controls status in both the vector returned during an interrupt acknowledge cycle and the status in RR2B. This bit is reset by a hardware reset.

Table 5-6. Interrupt Vector Modification

V3	V2	V1	Status High/Status Low =0
V4	V5	V6	Status High/Status Low =1
0	0	0	Ch B Transmit Buffer Empty
0	0	1	Ch B External/Status Change
0	1	0	Ch B Receive Char. Available
0	1	1	Ch B Special Receive Condition
1	0	0	Ch A Transmit Buffer Empty
1	0	1	Ch A External/Status Change
1	1	0	Ch A Receive Char. Available
1	1	1	Ch A Special Receive Condition

Bit 3: Master Interrupt Enable

This bit is set to 1 to globally enable interrupts, and cleared to zero to disable interrupts. Clearing this bit to zero forces the IEO pin to follow the state of the IEI pin unless there is an IUS bit set in the SCC. No IUS bit is set after the MIE bit is cleared to zero. This bit is reset by a hardware reset.

Bit 2: Disable Lower Chain control bit

The Disable Lower Chain bit is used by the CPU to control the interrupt daisy chain. Setting this bit to 1 forces the IEO pin Low, preventing lower priority devices on the daisy chain from requesting interrupts. This bit is reset by a hardware reset.

Bit 1: No Vector select bit

The No Vector bit controls whether or not the SCC responds to an interrupt acknowledge cycle. This is done by placing a vector on the data bus if the SCC is the highest priority device requesting an interrupt. If this bit is set, no vector is returned; i.e., AD7-AD0 remains tri-stated during an interrupt acknowledge cycle, even if the SCC is the highest priority device requesting an interrupt.

Bit 0: Vector Includes Status control bit

The Vector Includes Status Bit controls whether or not the SCC includes status information in the vector it places on the bus in response to an interrupt acknowledge cycle. If this bit is set, the vector returned is variable, with the variable field depending on the highest priority IP that is set. Table 5-5 shows the encoding of the status information. This bit is ignored if the No Vector (NV) bit is set.

5.2.13 Write Register 10 (Miscellaneous Transmitter/Receiver Control Bits)

WR10 contains miscellaneous control bits for both the receiver and the transmitter. Bit positions for WR10 are shown in Figure 5-12. On the ESCC and 85C30 with the Extended Read option enabled, this register may be read as RR11.

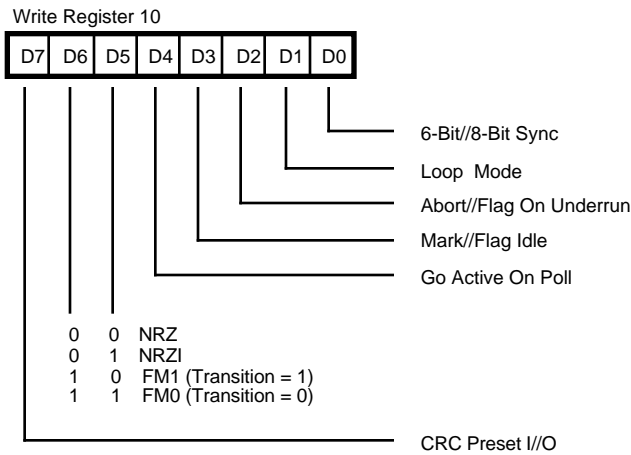


Figure 5-12. Write Register 10

Bit 7: CRC Presets I/O select bit

This bit specifies the initialized condition of the receive CRC checker and the transmit CRC generator. If this bit is set to 1, the CRC generator and checker are preset to 1. If this bit is set to 0, the CRC generator and checker are preset to 0. Either option can be selected with either CRC polynomial. In SDLC mode, the transmitted CRC is inverted before transmission, and the received CRC is checked against the bit pattern 0001110100001111. This bit is reset by a channel or hardware reset. This bit is ignored in Asynchronous mode.

Bits 6 and 5: Data Encoding select bits.

These bits control the coding method used for both the transmitter and the receiver, as illustrated in Table 5-7. All of the clocking options are available for all coding methods. The DPLL in the SCC is useful for recovering clocking information in NRZI and FM modes. Any coding method can be used in X1 mode. A hardware reset forces NRZ mode. Timing for the various modes is shown in Figure 5-13.

Table 5-7. Data Encoding

Bit 6	Bit 5	Encoding
0	0	NRZ
0	1	NRZI
1	0	FM1 (transition = 1)
1	1	FM0 (transition = 0)

5.1 INTRODUCTION (Continued)

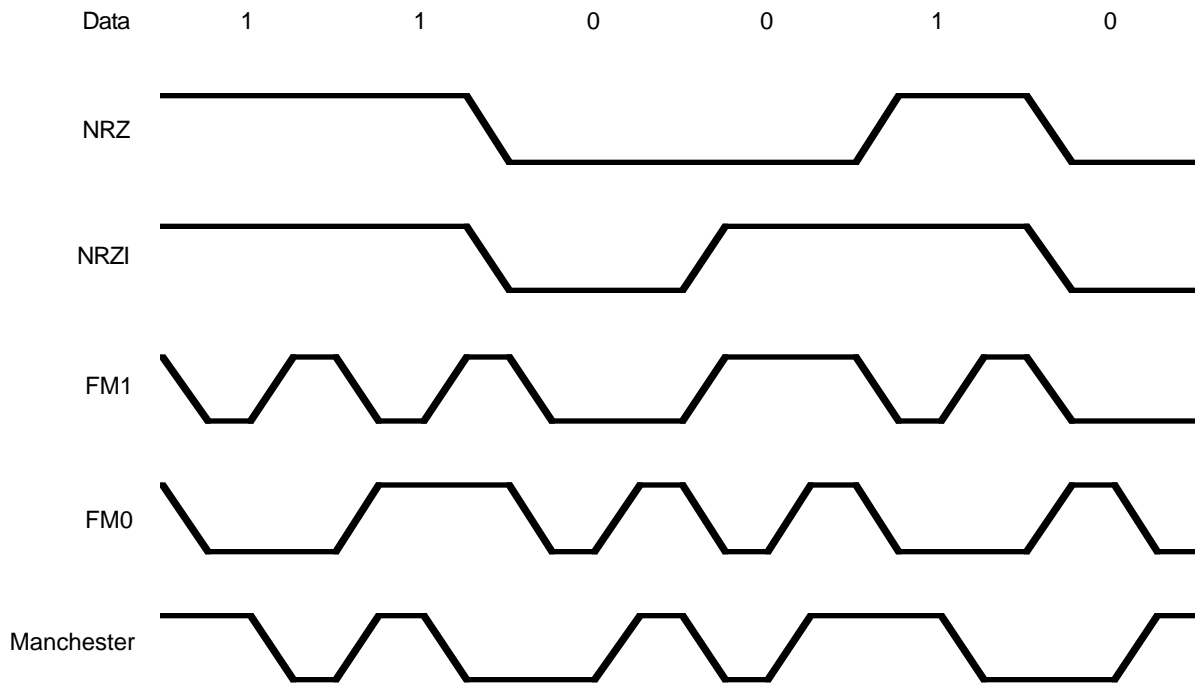


Figure 5-13. NRZ (NRZI), FM1 (FM0) Timing

Bit 4: Go-Active-On-Poll control bit

When Loop mode is first selected during SDLC operation, the SCC connects RxD to TxD with only gate delays in the path. The SCC does not go on-loop and insert the 1-bit delay between RxD and TxD until this bit has been set and an EOP received. When the SCC is on-loop, the transmitter does not go active unless this bit is set at the time an EOP is received. The SCC examines this bit whenever the transmitter is active in SDLC Loop mode and is sending a flag. If this bit is set at the time the flag is leaving the Transmit Shift register, another flag or data byte (if the transmit buffer is full) is transmitted.

If the Go-Active-On-Poll bit is not set at this time, the transmitter finishes sending the flag and reverts to the 1-Bit Delay mode. Thus, to transmit only one response frame, this bit is reset after the first data byte is sent to the SCC, but before CRC has been transmitted. If the bit is not reset before CRC is transmitted, extra flags are sent, slowing down response time on the loop. If this bit is reset before the first data is written, the SCC completes the transmission of the present flag and reverts to the 1-Bit Delay mode.

After gaining control of the loop, the SCC is not able to transmit again until a flag and another EOP are received. It is good practice to set this bit only upon receipt of a poll

frame to ensure that the SCC does not go on-loop without the CPU noticing it.

In synchronous modes other than SDLC with the Loop Mode bit set, this bit is set before the transmitter goes active in response to a received sync character.

This bit is always ignored in Asynchronous mode and Synchronous modes unless the Loop Mode bit is set. This bit is reset by a channel or hardware reset.

Bit 3: Mark//Flag Idle line control bit

This bit affects only SDLC operation and is used to control the idle line condition. If this bit is set to 0, the transmitter send flags as an idle line. If this bit is set to 1, the transmitter sends continuous 1s after the closing flag of a frame. The idle line condition is selected byte by byte i.e., either a flag or eight 1s are transmitted. The primary station in an SDLC loop should be programmed for Mark Idle to create the EOP sequence. Mark Idle must be deselected at the beginning of a frame before the first data is written to the SCC, so that an opening flag is transmitted. This bit is ignored in Loop mode, but the programmed value takes effect upon exiting the Loop mode. This bit is reset by a channel or hardware reset.

On the ESCC and 85C30 with the Automatic TX SDLC Flag mode enabled (WR7', D0=1), this bit can be left as mark idle. It will send an opening flag automatically, as well as sending a closing flag followed by mark idle after the frame transmission is completed.

Bit 2: Abort//Flag On Underrun select bit

This bit affects only SDLC operation and is used to control how the SCC responds to a transmit underrun condition. If this bit is set to 1 and a transmit underrun occurs, the SCC sends an abort and a flag instead of a CRC. If this bit is reset, the SCC sends a CRC on a transmit underrun. At the beginning of this 16-bit transmission, the Transmit Underrun/EOM bit is set, causing an External/Status interrupt. The CPU uses this status, along with the byte count from memory or the DMA, to determine whether the frame must be retransmitted.

To start the next frame, a Transmit Buffer Empty interrupt occurs at the end of this 16-bit transmission. If both this bit and the Mark/Flag Idle bit are set to 1, all 1s are transmitted after the transmit underrun. This bit should be set after the first byte of data is sent to the SCC and reset immediately after the last byte of data, terminating the frame properly with CRC and a flag. This bit is ignored in Loop mode, but the programmed value is active upon exiting Loop mode. This bit is reset by a channel or hardware reset.

Bit 1: Loop Mode control bit

In SDLC mode, the initial set condition of this bit forces the SCC to connect TxD to RxD and to begin searching the incoming data stream so that it can go on loop. All bits pertinent to SDLC mode operation in other registers are set before this mode is selected. The transmitter and receiver are not enabled until after this mode has been selected. As soon as the Go-Active-On-Poll bit is set and an EOP is received, the SCC goes on-loop. If this bit is reset after the SCC goes on-loop, the SCC waits for the next EOP to go off-loop.

In synchronous modes, the SCC uses this bit, along with the Go-Active-On-Poll bit, to synchronize the transmitter to the receiver. The receiver should not be enabled until after this mode is selected. The TxD pin is held marking when this mode is selected unless a break condition is programmed. The receiver waits for a sync character to be received and then enables the transmitter on a character boundary. The break condition, if programmed, is removed. This mode works properly with sync characters of 6, 8, or 16 bits. This bit is ignored in Asynchronous mode and is reset by a channel or hardware reset.

Bit 0: 6-Bit/8-Bit SYNC select bit

This bit is used to select a special case of synchronous modes. If this bit is set to 1 in Monosync mode, the receiver and transmitter sync characters are six bits long instead of the usual eight. If this bit is set to 1 in Bisync mode, the received sync is 12 bits and the transmitter sync character remains 16 bits long. This bit is ignored in

SDLC and Asynchronous modes, but still has effect in the special external sync modes. This bit is reset by a channel or hardware reset.

5.2.14 Write Register 11 (Clock Mode Control)

WR11 is the Clock Mode Control register. The bits in this register control the sources of both the receive and transmit clocks, the type of signal on the /SYNC and /RTxC pins, and the direction of the /TRxC pin. Bit positions for WR11 are shown in Figure 5-14; also, refer to Section 3.5 Clock Selection.

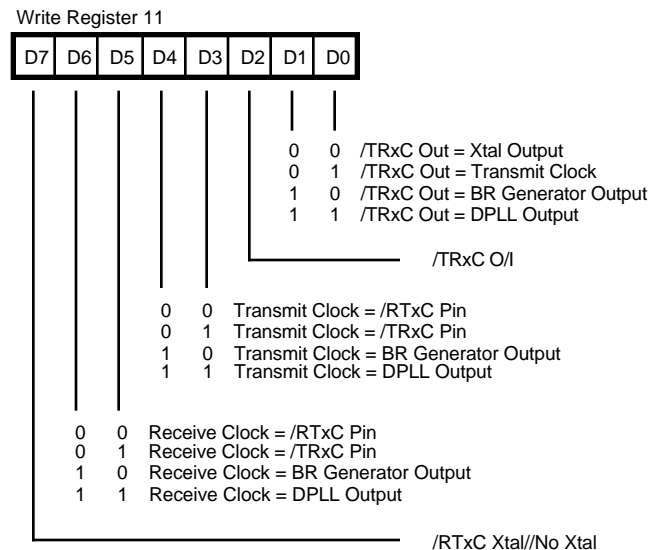


Figure 5-14. Write Register 11

Bit 7: RTxC-XTAL/NO XTAL select bit

This bit controls the type of input signal the SCC expects to see on the /RTxC pin. If this bit is set to 0, the SCC expects a TTL-compatible signal as an input to this pin. If this bit is set to 1, the SCC connects a high-gain amplifier between the /RTxC and /SYNC pins in expectation of a quartz crystal being placed across the pins.

The output of this oscillator is available for use as a clocking source. In this mode of operation, the /SYNC pin is unavailable for other use. The /SYNC signal is forced to zero internally. A hardware reset forces /NO XTAL. (At least 20 ms should be allowed after this bit is set to allow the oscillator to stabilize.)

Bits 6 and 5: Receiver Clock select bits 1 and 0

These bits determine the source of the receive clock as shown in Table 5-8. They do not interfere with any of the modes of operation in the SCC, but simply control a multiplexer just before the internal receive clock input. A hardware reset forces the receive clock to come from the /RTxC pin.

5.1 INTRODUCTION (Continued)

Table 5-8. Receive Clock Source

Bit 6	Bit 5	Receive Clock
0	0	/RTxC Pin
0	1	/TRxC Pin
1	0	BR Output
1	1	DPLL Output

Bits 4 and 3: Transmit Clock select bits 1 and 0.

These bits determine the source of the transmit clock as shown in Table 5-9. They do not interfere with any of the modes of operation of the SCC, but simply control a multiplexer just before the internal transmit clock input. The DPLL output that is used to feed the transmitter in FM modes lags by 90 degrees the output of the DPLL used by the receiver. This makes the received and transmitted bit cells occur simultaneously, neglecting delays. A hardware reset selects the /TRxC pin as the source of the transmit clocks.

Table 5-9. Transmit Clock Source

Bit 4	Bit 3	Transmit Clock
0	0	/RTxC Pin
0	1	/TRxC Pin
1	0	BR Output
1	1	DPLL Output

Bit 2: TRxC Pin I/O control bit

This bit determines the direction of the /TRxC pin. If this bit is set to 1, the /TRxC pin is an output and carries the signal selected by D1 and D0 of this register. However, if either the receive or the transmit clock is programmed to come from the /TRxC pin, /TRxC is an input, regardless of the state of this bit. The /TRxC pin is also an input if this bit is set to 0. A hardware reset forces this bit to 0.

Bits 1 and 0: /TRxC Output Source select bits 1 and 0

These bits determine the signal to be echoed out of the SCC via the /TRxC pin as given in Table 5-10. No signal is produced if /TRxC has been programmed as the source of either the receive or the transmit clock. If /TRxC O/I (bit 2) is set to 0, these bits are ignored.

If the XTAL oscillator output is programmed to be echoed, and the XTAL oscillator is not enabled, the /TRxC pin goes High. The DPLL signal that is echoed is the DPLL signal

used by the receiver. Hardware reset selects the XTAL oscillator as the output source.

Table 5-10. Transmit External Control Selection

Bit 1	Bit 0	TRxC Pin Output
0	0	XTAL Oscillator Output
0	1	Transmit Clock
1	0	BR Output
1	1	DPLL Output (receive)

5.2.15 Write Register 12 (Lower Byte of Baud Rate Generator Time Constant)

WR12 contains the lower byte of the time constant for the baud rate generator. The time constant can be changed at any time, but the new value does not take effect until the next time the time constant is loaded into the down counter. No attempt is made to synchronize the loading of the time constant into WR12 and WR13 with the clock driving the down counter. For this reason, it is advisable to disable the baud rate generator while the new time constant is loaded into WR12 and WR13. Ordinarily, this is done anyway to prevent a load of the down counter between the writing of the upper and lower bytes of the time constant.

The formula for determining the appropriate time constant for a given baud is shown below, with the desired rate in bits per second and the BR clock period in seconds. This formula is derived because the counter decrements from N down to zero-plus-one-cycle for reloading the time constant. This is then fed to a toggle flip-flop to make the output a square wave. Bit positions for WR12 are shown in Figure 5-15.

$$\text{Time Constant} = \frac{\text{Clock Frequency}}{2 \times (\text{Desired Rate}) \times (\text{BR Clock Period})} - 2$$

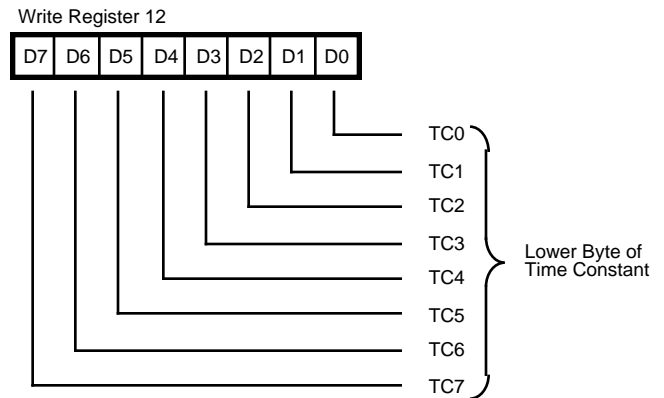


Figure 5-15. Write Register 12

5.2.16 Write Register 13 (Upper Byte of Baud Rate Generator Time Constant)

WR13 contains the upper byte of the time constant for the baud rate generator. Bit positions for WR13 are shown in Figure 5-16.

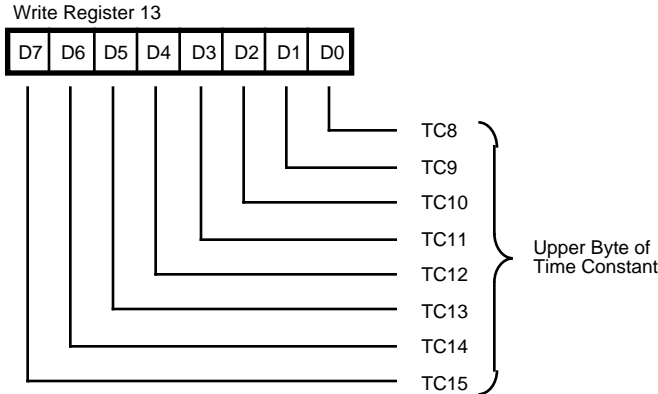


Figure 5-16. Write Register 13

5.2.17 Write Register 14 (Miscellaneous Control Bits)

WR14 contains some miscellaneous control bits. Bit positions for WR14 are shown in Figure 5-17. For DPLL function, refer to section 3.4 as well.

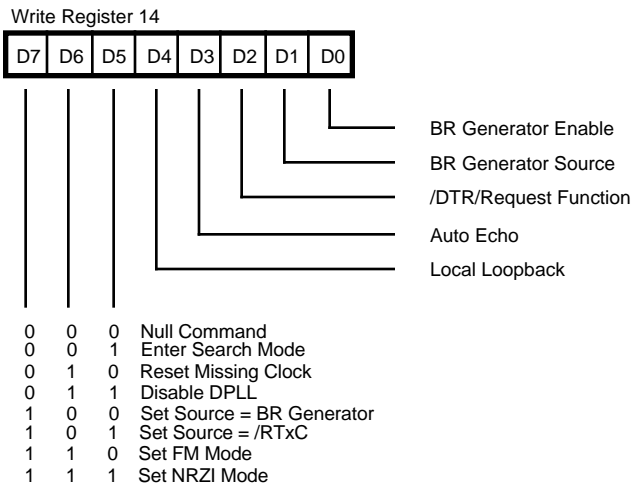


Figure 5-17. Write Register 14

Bits D7-D5: Digital Phase-Locked Loop Command Bits.

These three bits encode the eight commands for the Digital Phase-Locked Loop. A channel or hardware reset disables the DPLL, resets the missing clock latches, sets the

source to the /RTxC pin and selects NRZI mode. The Enter Search Mode command enables the DPLL after a reset.

Null Command (000). This command has no effect on the DPLL.

Enter Search Mode Command (001). Issuing this command causes the DPLL to enter the Search mode, where the DPLL searches for a locking edge in the incoming data stream. The action taken by the DPLL upon receipt of this command depends on the operating mode of the DPLL.

In NRZI mode, the output of the DPLL is High while the DPLL is waiting for an edge in the incoming data stream. After the Search mode is entered, the first edge the DPLL sees is assumed to be a valid data edge, and the DPLL begins the clock recovery operation from that point. The DPLL clock rate must be 32x the data rate in NRZI mode. Upon leaving the Search mode, the first sampling edge of the DPLL occurs 16 of these 32x clocks after the first data edge, and the second sampling occurs 48 of these 32x clocks after the first data edge. Beyond this point, the DPLL begins normal operation, adjusting the output to remain in sync with the incoming data.

In FM mode, the output of the DPLL is Low while the DPLL is waiting for an edge in the incoming data stream. The first edge the DPLL detects is assumed to be a valid clock edge. For this to be the case, the line must contain only clock edges; i.e. with FM1 encoding, the line must be continuous 0s. With FM0 encoding the line must be continuous 1s, whereas Manchester encoding requires alternating 1s and 0s on the line. The DPLL clock rate must be 16 times the data rate in FM mode. The DPLL output causes the receiver to sample the data stream in the nominal center of the two halves of the bit to decide whether the data was a 1 or a 0.

After this command is issued, as in NRZI mode, the DPLL starts sampling immediately after the first edge is detected. (In FM mode, the DPLL examines the clock edge of every other bit to decide what correction must be made to remain in sync.) If the DPLL does not see an edge during the expected window, the one clock missing bit in RR10 is set. If the DPLL does not see an edge after two successive attempts, the two clocks missing bits in RR10 are set and the DPLL automatically enters the Search mode. This command resets both clocks missing latches.

Reset Clock Missing Command (010). Issuing this command disables the DPLL, resets the clock missing latches in RR10, and forces a continuous Search mode state.

Disable DPLL Command (011). Issuing this command disables the DPLL, resets the clock missing latches in RR10, and forces a continuous Search mode state.

5.1 INTRODUCTION (Continued)

Set Source to BRG Command (100). Issuing this command forces the clock for the DPLL to come from the output of the BRG.

Set Source to /RTxC Command (101). Issuing the command forces the clock for the DPLL to come from the /RTxC pin or the crystal oscillator, depending on the state of the XTAL/no XTAL bit in WR11. This mode is selected by a channel or hardware reset.

Set FM Mode Command (110). This command forces the DPLL to operate in the FM mode and is used to recover the clock from FM or Manchester-Encoded data. (Manchester is decoded by placing the receiver in NRZ mode while the DPLL is in FM mode.)

Set NRZI Mode Command (111). Issuing this command forces the DPLL to operate in the NRZI mode. This mode is also selected by a hardware or channel reset.

Bit 4: Local Loopback select bit

Setting this bit to 1 selects the Local Loopback mode of operation. In this mode, the internal transmitted data is routed back to the receiver, and to the TxD pin. The /CTS and /DCD inputs are ignored as enables in Local Loopback mode, even if auto enable is selected. (If so programmed, transitions on these inputs still cause interrupts.) This mode works with any Transmit/Receive mode except Loop mode. For meaningful results, the frequency of the transmit and receive clocks must be the same. This bit is reset by a channel or hardware reset.

Bit 3: Auto Echo select bit

Setting this bit to 1 selects the Auto Echo mode of operation. In this mode, the TxD pin is connected to RxD as in Local Loopback mode, but the receiver still listens to the RxD input. Transmitted data is never seen inside or outside the SCC in this mode, and /CTS is ignored as a transmit enable. This bit is reset by a channel or hardware reset.

Bit 2: DTR/Request Function select bit

This bit selects the function of the /DTR//REQ pin following the state of the DTR bit in WR5. If this is set to 0, the /DTR//REQ pin follows the state of the DTR bit in WR5. If this bit is set to 1, the /DTR//REQ pin goes Low whenever the transmit buffer becomes empty and in any of the synchronous modes when the CRC has been sent at the end of a message. The request function on the /DTR//REQ pin differs from the transmit request function available on the /W//REQ pin. The /REQ does not go inactive until the internal operation satisfying the request is complete, which occurs three to four PCLK cycles after the falling edge of /DS, /RD or /WR. If the DMA used is edge-triggered, this difference is unimportant. The deassertion timing of the REQ mode can be programmed to occur with the same timing

as the /W//REQ pin if WR7' D4=1. This bit is reset by a channel or hardware reset.

Bit 1: Baud Rate Generator Source select bit

This bit selects the source of the clock for the baud rate generator. If this bit is set to 0. The baud rate generator clock comes from either the /RTxC pin or the XTAL oscillator (depending on the state of the XTAL/no XTAL bit). If this bit is set to 1, the clock for the baud rate generator is the SCC's PCLK input. Hardware reset sets this bit to 0, select the /RTxC pin as the clock source for the BRG.

Bit 0: Baud Rate Generator Enable

This bit controls the operation of the BRG. The counter in the BRG is enabled for counting when this bit is set to 1, and counting is inhibited when this bit is set to 0. When this bit is set to 1, change in the state of this bit is not reflected by the output of the BRG for two counts of the counter. This allows the command to be synchronized. However, when set to 0, disabling is immediate. This bit is reset by a hardware reset.

5.2.18 Write Register 15 (External/Status Interrupt Control)

WR15 is the External/Status Source Control register. If the External/Status interrupts are enabled as a group via WR1, bits in this register control which External/Status conditions cause an interrupt. Only the External/Status conditions that occur after the controlling bit is set to 1 cause an interrupt. This is true, even if an External/Status condition is pending at the time the bit is set. Bit positions for WR15 are shown in Figure 5-18.

On the CMOS version, bits D2 and D0 are reserved. On the NMOS version, bit D2 is reserved. These reserved bits should be written as 0s.

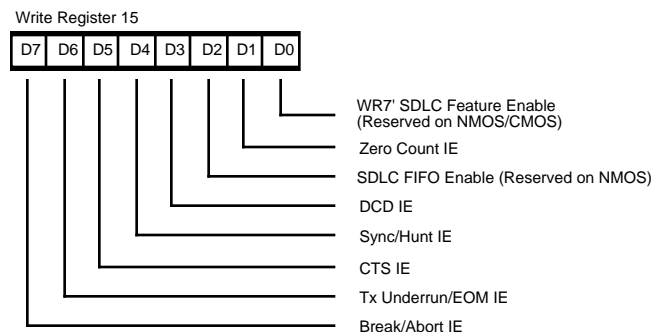


Figure 5-18. Write Register 15

Bit 7: Brea/Abort Interrupt Enable

If this bit is set to 1, a change in the Break/Abort status of the receiver causes an External/Status interrupt. This bit is set by a channel or hardware reset.

Bit 6: Transmit Underrun/EOM Interrupt Enable

If this bit is set to 1, a change of state by the Tx Underrun/EOM latch in the transmitter causes an External/Status interrupt. This bit is set to 1 by a channel or hardware reset.

Bit 5: CTS Interrupt Enable

If this bit is set to 1, a change of state on the /CTS pin causes an External/Status Interrupt. This bit is set by a channel or hardware reset.

Bit 4: SYNC/Hunt Interrupt Enable

If this bit is set to 1, a change of state on the /SYNC pin causes an External/Status interrupt in Asynchronous mode, and a change of state in the Hunt bit in the receiver causes and External/Status interrupt in synchronous modes. This bit is set by a channel or hardware reset.

Bit 3: DCD Interrupt Enable

If this bit is set to 1, a change of state on the /DCD pin causes an External/Status interrupt. This bit is set by a channel or hardware reset.

Bit 2: Status FIFO Enable control bit (CMOS/ESCC)

If this bit is set and if the CMOS/ESCC is in the SDLC/HDLC Mode, status (five bits from Read Register 1:

Residue, Overrun, and CRC Error) and fourteen bits of byte count are held in the Status FIFO until read. Status information for up to ten frames can be stored. If this bit is reset (0) or if the CMOS/ESCC is not in the SDLC/HDLC Mode, the FIFO is not operational and status information read reflects the current status only. This bit is reset to 0 by a channel or hardware reset. For details on this function, refer to Section 4.4.3.

On the NMOS version, this bit is reserved and should be programmed as 0.

Bit 1: Zero Count Interrupt Enable

If this bit is set to 1, an External/Status interrupt is generated whenever the counter in the baud rate generator reaches 0. This bit is reset to 0 by a channel or hardware reset.

Bit 0: Point to Write Register WR7 Prime (ESCC and 85C30 only)

When this bit is programmed to 0, writes to the WR7 address are made to WR7. When this bit is programmed to 1, writes to the WR7 address are made to WR7 Prime. Once set, this bit remains set unless cleared by writing a 0 to this bit or by a hardware or software reset. Note that if the extended read option is enabled, WR7 Prime is read in RR14. For details about WR7', refer to Section 4.4.1.2 and Section 5.2.9.

On the NMOS/CMOS version, this bit is reserved and should be programmed as 0.

5.3 READ REGISTERS

The SCC Read register set in each channel has four status registers (includes receive data FIFO), and two baud rate time constant registers in each channel. The Interrupt Vector register (RR2) and Interrupt Pending register (RR3) are shared by both channels. In addition to these, the CMOS/ESCC has two additional registers for the SDLC Frame Status FIFO. On the ESCC, if that function is enabled (WR7' bit D6=1), five more registers are available which return the value written to the write registers.

The status of these registers is continually changing and depends on the mode of communication, received and transmitted data, and the manner in which this data is transferred to and from the CPU. The following description details the bit assignment for each register.

5.3.1 Read Register 0 (Transmit/Receive Buffer Status and External Status)

Read Register 0 (RR0) contains the status of the receive and transmit buffers. RR0 also contains the status bits for the six sources of External/Status interrupts. The bit configuration is illustrated in Figure 5-19.

On the NMOS/CMOS version, note that the status of this register might be changing during the read.

An enhancement allows the ESCC and 85C30 to latch the contents of RR0 during read transactions for this register. The latch is released on the rising edge of the /RD of the read transaction to this register. This feature prevents missed status due to changes that take place when the read cycle is in progress.

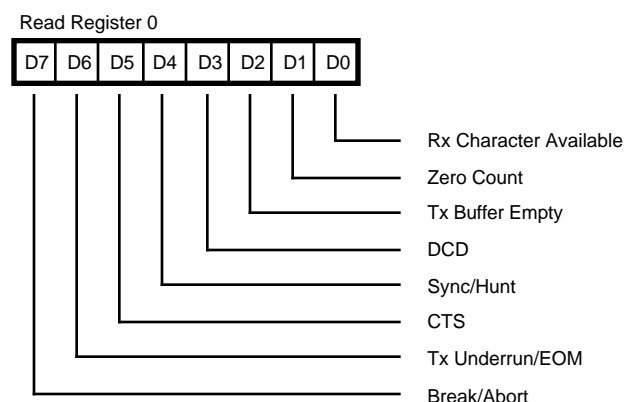


Figure 5-19. Read Register 0

5.3 READ REGISTERS (Continued)

Bit 7: Break/Abort status

In the Asynchronous mode, this bit is set when a Break sequence (null character plus framing error) is detected in the receive data stream. This bit is reset when the sequence is terminated, leaving a single null character in the Receive FIFO. This character is read and discarded. In SDLC mode, this bit is set by the detection of an Abort sequence (seven or more 1s), then reset automatically at the termination of the Abort sequence. In either case, if the Break/Abort IE bit is set, an External/Status interrupt is initiated. Unlike the remainder of the External/Status bits, both transitions are guaranteed to cause an External/Status interrupt, even if another External/Status interrupt is pending at the time these transitions occur. This procedure is necessary because Abort or Break conditions may not persist.

Bit 6: Transmit Underrun/EOM status

This bit is set by a channel or hardware reset when the transmitter is disabled or a Send Abort command is issued. This bit is only reset by the reset Tx Underrun/EOM Latch command in WR0. When the Transmit Underrun occurs, this bit is set and causes an External/Status interrupt (if the Tx Underrun/EOM IE bit is set).

Only the 0-to-1 transition of this bit causes an interrupt. This bit is always 1 in Asynchronous mode, unless a reset Tx Underrun/EOM Latch command has been erroneously issued. In this case, the Send Abort command can be used to set the bit to one and at the same time cause an External/Status interrupt.

Bit 5: Clear to Send pin status

If the CTS IE bit in WR15 is set, this bit indicates the state of the /CTS pin while no interrupt is pending, latches the state of the /CTS pin and generates an External/Status interrupt. Any odd number of transitions on the /CTS pin causes another External/Status interrupt condition. If the CTS IE bit is reset, it merely reports the current unlatched state of the /CTS pin.

Bit 4: Sync/Hunt status

The operation of this bit is similar to that of the CTS bit, except that the condition monitored by the bit varies depending on the mode in which the SCC is operating.

When the XTAL oscillator option is selected in asynchronous modes, this bit is forced to 0 (no External/Status interrupt is generated). Selecting the XTAL oscillator in synchronous or SDLC modes has no effect on the operation of this bit.

The XTAL oscillator should not be selected in External Sync mode.

In Asynchronous mode, the operation of this bit is identical to that of the CTS status bit, except that this bit reports the state of the /SYNC pin.

In External sync mode the /SYNC pin is used by external logic to signal character synchronization. When the Enter Hunt Mode command is issued in External Sync mode, the /SYNC pin must be held High by the external sync logic until character synchronization is achieved. A High on the /SYNC pin holds the Sync/Hunt bit in the reset condition.

When external synchronization is achieved, /SYNC is driven Low on the second rising edge of the Receive Clock after the last rising edge of the Receive Clock on which the last bit of the receive character was received. Once /SYNC is forced Low, it is good practice to keep it Low until the CPU informs the external sync logic that synchronization is lost or that a new message is about to start. Both transitions on the /SYNC pin cause External/Status interrupts if the Sync/Hunt IE bit is set to 1.

The Enter Hunt Mode command should be issued whenever character synchronization is lost. At the same time, the CPU should inform the external logic that character synchronization has been lost and that the SCC is waiting for /SYNC to become active.

In the Monosync and Bisync Receive modes, the Sync/Hunt status bit is initially set to 1 by the Enter Hunt Mode command. The Sync/Hunt bit is reset when the SCC established character synchronization. Both transitions cause External/Status interrupts if the Sync/Hunt IE bit is set. When the CPU detects the end of message or the loss of character synchronization, the Enter Hunt Mode command should be issued to set the Sync/Hunt bit and cause an External/Status interrupt. In this mode, the /SYNC pin is an output, which goes Low every time a sync pattern is detected in the data stream.

In the SDLC modes, the Sync/Hunt bit is initially set by the Enter Hunt Mode command or when the receiver is disabled. It is reset when the opening flag of the first frame is detected by the SCC. An External/Status interrupt is also generated if the Sync/Hunt IE bit is set. Unlike the Monosync and Bisync modes, once the Sync/Hunt bit is reset in SDLC mode, it does not need to be set when the end of the frame is detected. The SCC automatically maintains synchronization. The only way the Sync/Hunt bit is set again is by the Enter Hunt Mode command or by disabling the receiver.

Bit 3: Data Carrier Detect status

If the DCD IE bit in WR15 is set, this bit indicates the state of the /DCD pin the last time the Enabled External/Status bits changed. Any transition on the /DCD pin, while no interrupt is pending, latches the state of the /DCD pin and

generates an External/Status interrupt. Any odd number of transitions on the /DCD pin while another External/Status interrupt condition. If the DCD IE is reset, this bit merely reports the current, unlatched state of the /DCD pin.

Bit 2: TX Buffer Empty status

This bit is set to 1 when the transmit buffer is empty. It is reset while the CRC is sent in a synchronous or SDLC mode and while the transmit buffer is full. The bit is reset when a character is loaded into the transmit buffer.

On the ESCC, the status of this bit is not related to the Transmit Interrupt Status or the state of WR7' bit D5, but it shows the status of the entry location of the Transmit FIFO. This means more data can be written without being overwritten. This bit is set to 1 when the entry location of the Transmit FIFO is empty. It is reset when a character is loaded into the entry location of the Transmit FIFO.

This bit is always in the set condition after a hardware or channel reset.

For more information on this bit, refer to Section 2.4.8 "Transmit Interrupts and Transmit Buffer Empty bit".

Bit 1: Zero Count status

If the Zero Count interrupt Enable bit is set in WR15, this bit is set to one while the counter in the baud rate generator is at the count of zero. If there is no other External/Status interrupt condition pending at the time this bit is set, an External/Status interrupt is generated. However, if there is another External/Status interrupt pending at this time, no interrupt is initiated until interrupt service is complete. If the Zero Count condition does not persist beyond the end of the interrupt service routine, no interrupt is generated. This bit is not latched High, even though the other External/Status latches close as a result of the Low-to-High transition on ZC. The interrupt routine checks the other External/Status conditions for changes. If none changed, ZC was the source. In polled applications, check the IP bit in RR3A for a status change and then proceed as in the interrupt service routine.

Bit 0: Receive Character Available

This bit is set to 1 when at least one character is available in the receive data FIFO. It is reset when the receive data FIFO is completely empty. A channel or hardware reset empties the receive data FIFO.

On the ESCC, the status of this bit is independent of WR7' bit D3.

For details on this bit, refer to Section 2.4.7, The Receive Interrupt.

5.3.2 Read Register 1

RR1 contains the Special Receive Condition status bits and the residue codes for the I-field in SDLC mode. Figure 5-20 shows the bit positions for RR1.

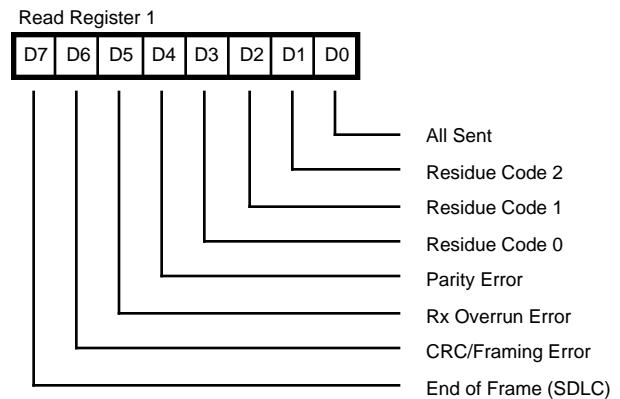


Figure 5-20. Read Register 1

Bit 7: End of Frame (SDLC) status

This bit is used only in SDLC mode and indicates that a valid closing flag has been received and that the CRC Error bit and residue codes are valid. This bit is reset by issuing the Error Reset command. It is also updated by the first character of the following frame. This bit is reset in any mode other than SDLC.

Bit 6: CRC/Framing Error status

If a framing error occurs (in Asynchronous mode), this bit is set (and not latched) for the receive character in which the framing error occurred. Detection of a framing error adds an additional one-half bit to the character time so that the framing error is not interpreted as a new Start bit. In Synchronous and SDLC modes, this bit indicates the result of comparing the CRC checker to the appropriate check value. This bit is reset by issuing an Error Reset command, but the bit is never latched. Therefore, it is always updated when the next character is received. When used for CRC error status in Synchronous or SDLC modes, this bit is usually set since most bit combinations, except for a correctly completed message, result in a non-zero CRC.

On the CMOS and ESCC, if the Status FIFO is enabled (refer to the description in Write Register 15, bit D2 and the description in Read Register 7, bits D7 and D6), this bit reflects the status stored at the exit location of the Status FIFO.

Bit 5: Receiver Overrun Error status

This bit indicates that the Receive FIFO has overflowed. Only the character that has been written over is flagged with this error. When that character is read, the Error condition is latched until reset by the Error Reset command.

5.3 READ REGISTERS (Continued)

Also, a Special Receive Condition vector is returned, caused by the overrun characters and all subsequent characters received until the Error Reset command is issued.

On the CMOS and ESCC, if the Status FIFO is enabled (refer to the description in Write Register 15, bit D2 and the description in Read Register 7, bits D7 and D6), this bit reflects the status stored at the exit location of the Status FIFO.

Bit 4: Parity Error status.

When parity is enabled, this bit is set for the characters whose parity does not match the programmed sense (even/odd). This bit is latched so that once an error occurs, it remains set until the Error Reset command is issued. If the parity in Special Condition bit is set, a parity error causes a Special Receive Condition vector to be returned on the character containing the error and on all subsequent characters until the Error Reset command is issued.

Bits 3, 2, and 1: Residue Codes, bits 2, 1, and 0

In those cases in SDLC mode where the received I-Field

is not an integral multiple of the character length, these three bits indicate the length of the I-Field and are meaningful only for the transfer in which the end of frame bit is set. This field is set to 011 by a channel or hardware reset and is forced to this state in Asynchronous mode. These three bits can leave this state only if SDLC is selected and a character is received. The codes signify the following (Reference Table 5-11) when a receive character length is eight bits per character.

On the CMOS and ESCC, if the Status FIFO is enabled (refer to the description in Write Register 15, bit D2 and the description in Read Register 7, bits D7 and D6), these bits reflect the status stored at the exit location of the Status FIFO.

I-Field bits are right-justified in all cases. If a receive character length other than eight bits is used for the I-Field, a table similar to Table 5-11 can be constructed for each different character length. Table 5-12 shows the residue codes for no residue (The I-Field boundary lies on a character boundary).

Table 5-11. I-Field Bit Selection (8 Bits Only)

Bit 3	Bit 2	Bit 1	I-Field Bits in Last Byte	I-Field Bits in Previous Byte
1	0	0	0	3
0	1	0	0	4
1	1	0	0	5
0	0	1	0	6
1	0	1	0	7
0	1	1	0	8
1	1	1	1	8
0	0	0	2	8

Table 5-12. Bits per Character Residue Decoding

Bits per Character	Bit 3	Bit 2	Bit 1
8	0	1	1
7	0	0	0
6	0	1	0
5	0	0	1

Bit 0: All Sent status

In Asynchronous mode, this bit is set when all characters have completely cleared the transmitter pins. Most modems contain additional delays in the data path, which requires the modem control signals to remain active until after the data has cleared both the transmitter and the modem. This bit is always set in synchronous and SDLC modes.

5.3.3 Read Register 2

RR2 contains the interrupt vector written into WR2. When the register is accessed in Channel A, the vector returned is the vector actually stored in WR2. When this register is accessed in Channel B, the vector returned includes status information in bits 1, 2 and 3 or in bits 6, 5 and 4, depending on the state of the Status High/Status Low bit in WR9 and independent of the state of the VIS bit in WR9. The vector is modified according to Table 5-6 shown in the explanation of the VIS bit in WR9 (Section 5.2.11). If no interrupts are pending, the status is V3,V2,V1 -011, or V6,V5,V4-110. Figure 5-21 shows the bit positions for RR2.

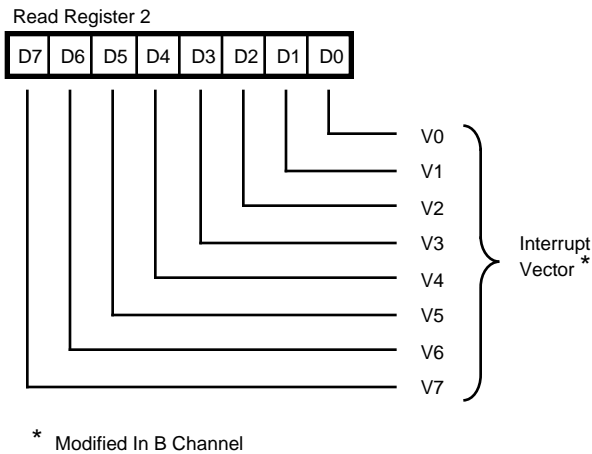


Figure 5-21. Read Register 2

5.3.4 Read Register 3

RR3 is the interrupt Pending register. The status of each of the interrupt Pending bits in the SCC is reported in this register. This register exists only in Channel A. If this register is accessed in Channel B, all 0s are returned. The two unused bits are always returned as 0. Figure 5-22 shows the bit positions for RR3.

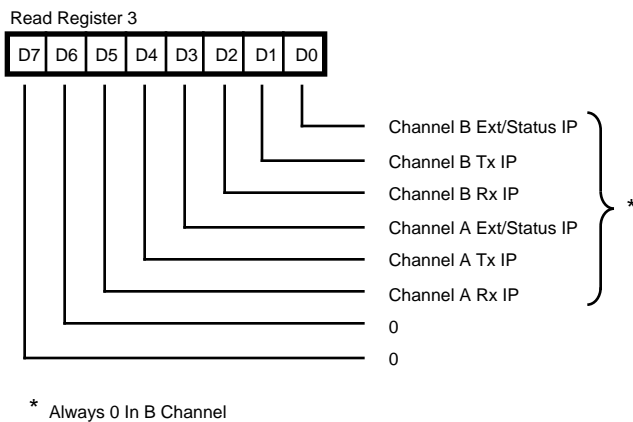


Figure 5-22. Read Register 3

5.3.5 Read Register 4 (ESCC and 85C30 Only)

On the ESCC, Read Register 4 reflects the contents of Write Register 4 provided the Extended Read option is enabled. Otherwise, this register returns an image of RR0.

On the NMOS/CMOS version, a read to this location returns an image of RR0.

5.3.6 Read Register 5 (ESCC and 85C30 Only)

On the ESCC, Read Register 5 reflects the contents of Write Register 5 provided the Extended Read option is enabled. Otherwise, this register returns an image of RR1.

On the NMOS/CMOS version, a read to this register returns an image of RR1.

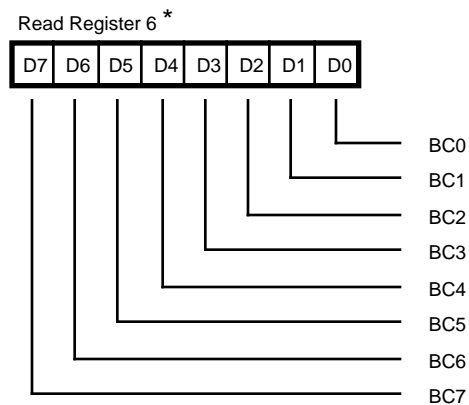
5.3.7 Read Register 6 (Not on NMOS)

On the CMOS and ESCC, Read Register 6 contains the least significant byte of the frame byte count that is currently at the top of the Status FIFO. RR6 is shown in Figure 5-23. This register is readable only if the FIFO is enabled (refer to the description Write Register 15, bit D2 and Section 4.4.3). Otherwise, this register is an image of RR2.

On the NMOS version, a read to this register location returns an image of RR2.

5.3.8 Read Register 7 (Not on NMOS)

On the CMOS and ESCC, Read Register 7 contains the most significant six bits of the frame byte count that is currently at the top of the Status FIFO. Bit D7 is the FIFO Overflow Status and bit D6 is the FIFO Data Available Status. The status indications are given in Table 5-13. RR7 is shown in Figure 5-24. This register is readable only if the FIFO is enabled (refer to the description Write Register 15, bit D2). Otherwise this register is an image of RR3. Note, for proper operation of the FIFO and byte count logic, the registers should be read in the following order: RR7, RR6, RR1.



SDLC FIFO Status and Byte Count (LSB)

Figure 5-23. Read Register 6 (Not on NMOS)

5.3 READ REGISTERS (Continued)

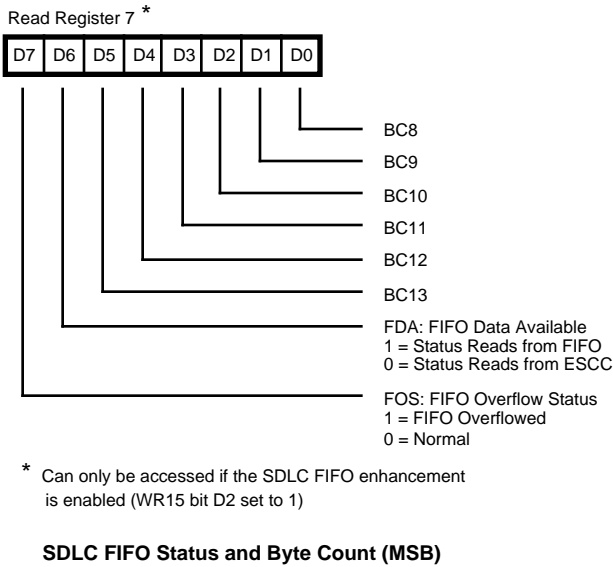


Figure 5-24. Read Register 7 (Not on NMOS)

Table 5-13. .Read Register 7 FIFO Status Decoding

Bit D7	FIFO Data Available Status
1	Status reads come from FIFO (FIFO is not Empty)
0	Status reads bypass FIFO because FIFO is Empty)
Bit D6	FIFO Overflow Status
1	FIFO has overflowed
0	Normal operation

If the FIFO overflows, the FIFO and the FIFO Overflow Status bit are cleared by disabling and then re-enabling the FIFO through the FIFO control bit (WR15, D2). Otherwise, this register returns an image of RR3.

On the NMOS version, a read to this location returns an image of RR3.

5.3.9 Read Register 8

RR8 is the Receive Data register.

5.3.10 Read Register 9 (ESCC and 85C30 Only)

On the ESCC, Read Register 9 reflects the contents of Write Register 3 provided the Extended Read option has been enabled.

On the NMOS/CMOS version, a read to this location returns an image of RR13.

5.3.11 Read Register 10

RR10 contains some miscellaneous status bits. Unused bits are always 0. Bit positions for RR10 are shown in Figure 5-25.

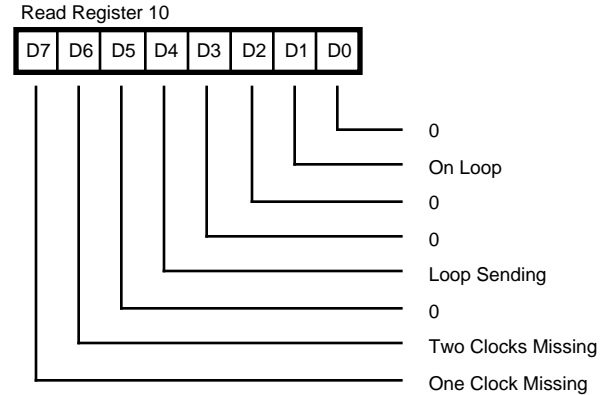


Figure 5-25. Read Register 10

Bit 7: One Clock Missing status

While operating in the FM mode, the DPLL sets this bit to 1 when it does not see a clock edge on the incoming lines in the window where it expects one. This bit is latched until reset by a Reset Missing Clock or Enter Search Mode command in WR14. In the NRZI mode of operation and while the DPLL is disabled, this bit is always 0.

Bit 6: Two Clocks Missing status

While operating in the FM mode, the DPLL sets this bit to 1 when it does not see a clock edge in two successive tries. At the same time the DPLL enters the Search mode. This bit is latched until reset by a Reset Missing Clock or Enter Search Mode command in WR14, bit 5-7. In the NRZI mode of operation and while the DPLL is disabled, this bit is always 0.

Bit 4: Loop Sending status

This bit is set to 1 in SDLC Loop mode while the transmitter is in control of the Loop, that is, while the SCC is actively transmitting on the loop. This bit is reset at all other times.

This bit can be polled in SDLC mode to determine when the closing flag has been sent.

Bit 1: On Loop status

This bit is set to 1 while the SCC is actually on loop in SDLC Loop mode. This bit is set to 1 in the X21 mode (Loop mode selected while in monosync) when the transmitter goes active. This bit is 0 at all other times. This bit can also be pulled in SDLC mode to determine when the closing flag has been sent.

5.3.12 Read Register 11 (ESCC and 85C30 Only)

On the ESCC, Read Register 11 reflects the contents of Write Register 10 provided the Extended Read option has been enabled. Otherwise, this register returns an image of RR15.

On the NMOS/CMOS version, a read to this location returns an image of RR15.

5.3.13 Read Register 12

RR12 returns the value stored in WR12, the lower byte of the time constant, for the BRG. Figure 5-26 shows the bit positions for RR12.

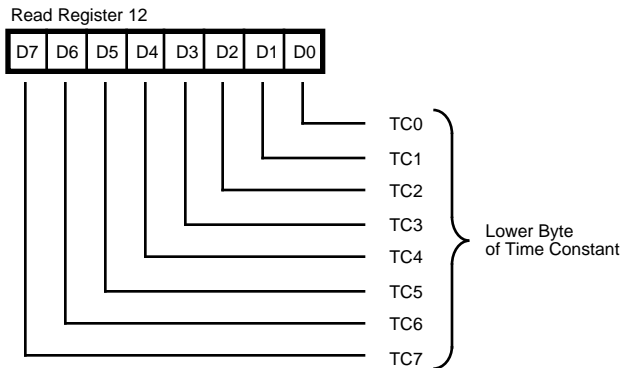


Figure 5-26. Read Register 12

5.3.14 Read Register 13

RR13 returns the value stored in WR13, the upper byte of the time constant for the BRG. Figure 5-27 shows the bit positions for RR13.

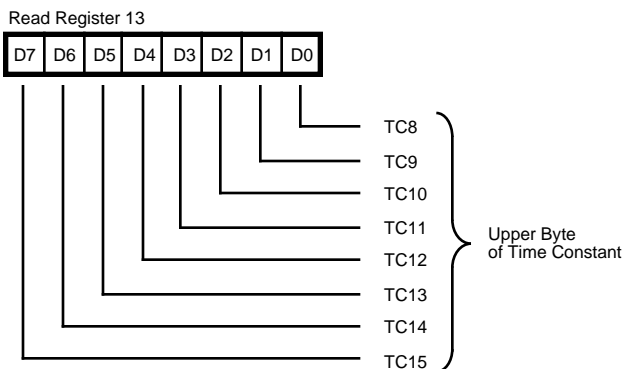


Figure 5-27. Read Register 13

5.3.15 Read Register 14 (ESCC and 85C30 Only)

On the ESCC, Read Register 14 reflects the contents of Write Register 7 Prime provided the Extended Read option has been enabled. Otherwise, this register returns an image of RR10.

On the NMOS/CMOS version, a read to this location returns an image of RR10.

5.3.16 Read Register 15

RR15 reflects the value stored in WR15, the External/Status IE bits. The two unused bits are always returned as Os. Figure 5-28 shows the bit positions for RR15.

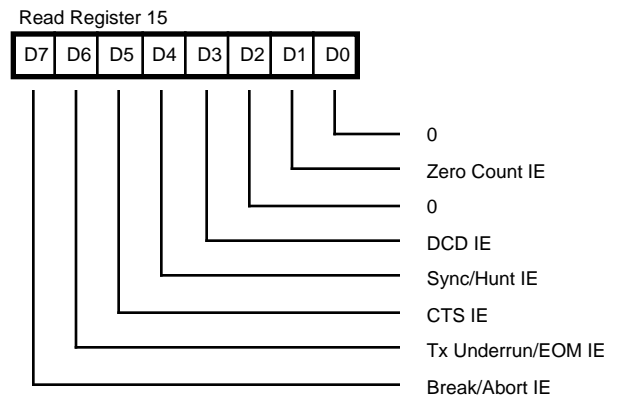


Figure 5-28. Read Register 15
